S5K3B2FA23

1/3.2” UXGA CMOS Image Sensor supporting SMIA 1.0

Preliminary Data Sheet

(Rev. 0.20)

DOCUMENT REVISION HISTORY

Versoin	Date	Amendment
0.00	06-02-13	Initial draft.
0.10	06-03-18	Page 9. Table 2. Module pin description changed for 16-Pin Module Page21. sec 2-2. Monotonicity of analog gain is stated. Page35. Table 8. I_{IL} test condition changed : VSS → DGND Page37. Table 9. EXTCLK frequency and amplitude specifications added CCP2 Skew parameters added Page38. Table 10. Design targets for “Latch-up” clarified Page39. Table 11. Min value for tLOW changed Page40. Table 12. Typical and Max values for “Image Lag” changed : (typ) 0.0001→ 0.001, (max) 0.0004 → 0.004 Page55. “Embedded Data Contents” is added.
0.20	06-04-18	Page11. Figure 4 : Pixel array information modified (shows active pixel area without color filters and micro lens)

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FEATURES

- SMIA 1.0 compliant
- Optical size: 1/3.2 inch
- Pixel size: 2.8 um
- Effective resolution: 1600 (H) x 1200 (V), UXGA
- Line progressive read out
- Vertical and horizontal flip mode
- Continuous frame capture mode
- Sub-sampled readout
- Output format: RAW 10-Bit and 8-Bit mode using DPCM/PCM compression
- Max. frame rate: 30fps @ UXGA (for all output format including RAW10)
- Digital gain control (X1~X8, 1/256 step)
- Color space conversion
- Image scaling down (to arbitrary number that is greater than or equal to 256x192)
- Built-in test pattern generation
- Standby mode for power saving
- CCI(I^2C-compatible) bus control interface
- Operating temperature: -30°C to +70°C
- Supply voltage: 2.8V for analog 1.8V for digital
- Internal voltage regulator for 1.5V generation
- Internal PLL for high speed clock generation
- High speed SubLVDS data/clock or data/strobe signaling

GENERAL DESCRIPTION

The S5K3B2FA is a highly integrated UXGA camera chip which includes CMOS image sensor (CIS) and CCP2-compliant image data interface. It is fabricated by SAMSUNG 0.13μm CMOS image sensor process developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor consists of 1600 x 1200 effective pixels which meet with 1/3.2 inch optical format. The CIS has on-chip 10-bit ADC arrays to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. The image data interface performs data formatting, image compression, Image scaling and serial transmission using SubLVDS. The host controller is able to access and control this device via CCI bus. The S5K3B2FA is suitable for low power camera module with 2.8V/1.8V power supply.

SMIA 95

9.5 X 9.5 X 7.6 (mm)

LOGICAL SYMBOL DIAGRAM

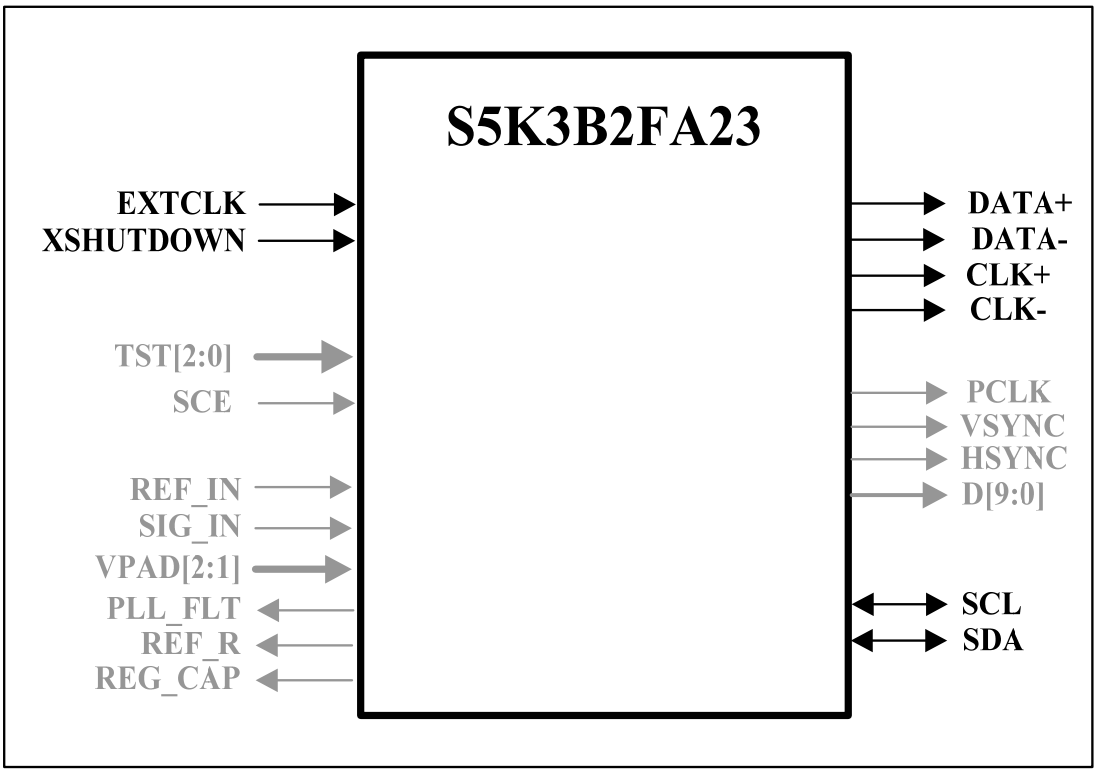


Figure 1 : Logical Symbol Diagram

CHIP PAD DESCRIPTION

Table 1 : Chip PAD Description

Pin No	Pin Name	I/O	Description
1	**NC (SIG_IN)**	I	No Connection (Signal input for ADC TEG test)
2	**NC (REF_IN)**	I	No Connection (Reference input for ADC TEG test)
3	**VPAD2**	I	Analog voltage PAD 2. External cap(0.1uF) connected to analog supply(2.8V)
4	**NC (VPAD1)**	I	No Connection (Analog voltage PAD 1)
7	**REF_R**	O	External reference resistor (12KΩ) connected to analog ground
8	**NC (VSS28_CCP)**	P	No Connection (Auxiliary analog ground)
9	**NC (VDD28_CCP)**	P	No Connection (Auxiliary analog power)
10,13	**NC (PLL_FLT)**	O	PLL loop filter voltage monitoring
15	**EXTCLK**	I	External input clock
17	**DATA+**	O	Differential CCP2 data signal (positive)
18	**DATA-**	O	Differential CCP2 data signal (negative)
21	**CLK+**	O	Differential CCP2 clock signal (positive)
22	**CLK-**	O	Differential CCP2 clock signal (negative)
25	**REG_CAP**	O	External cap (1uF) connected to digital ground
28	**XSHUTDOWN**	I	Active low shutdown signal
29	**SDA**	B	CCI data signal
30	**SCL**	B	CCI clock signal
31	**NC (TST0)**	I	No Connection (Control signal for test mode. internal pull-down)
32	**NC (TST1)**	I	No Connection (Control signal for test mode. internal pull-down)
33	**NC (TST2)**	I	No Connection (Control signal for test mode. internal pull-down)
34	**NC (SCE)**	I	No Connection (Control signal for test mode. internal pull-down)
35	**NC (HSYNC)**	O	No Connection (Horizontal sync output)
36	**NC (VSYNC)**	O	No Connection (Vertical sync output)
37	**NC (PCLK)**	O	No Connection (Pixel clock output)
38~40	**NC (D0~D2)**	O	No Connection (Parallel pixel data output. D0 : LSB, D9 : MSB)
45~51	**NC (D3~D9)**	O	
52	**NC (VSS18_DIG)**	P	No Connection (Auxiliary digital ground)
A1	**NC (TST_EFUSE)**	I	No Connection
A2	**NC (PD_REG)**	I	No Connection
A3~4	**NC (RX_CLK-/+)**	I	No Connection
A5~6	**NC (RX_DATA-/+)**	I	No Connection
A7	**NC (TCLK1)**	I	No Connection
A8	**NC (TCLK2)**	I	No Connection
6,9, 12,24	**VDD28_***	P	Analog Power (2.8V)
5,8, 11,23	**VSS28_***	P	Analog Ground
16,20, 27,43	**VDD18_***	P	Digital Power (1.8V)
14,19, 26,41, 42	**VSS18_***	P	Digital Ground

CHIP PAD CONFIGURATION

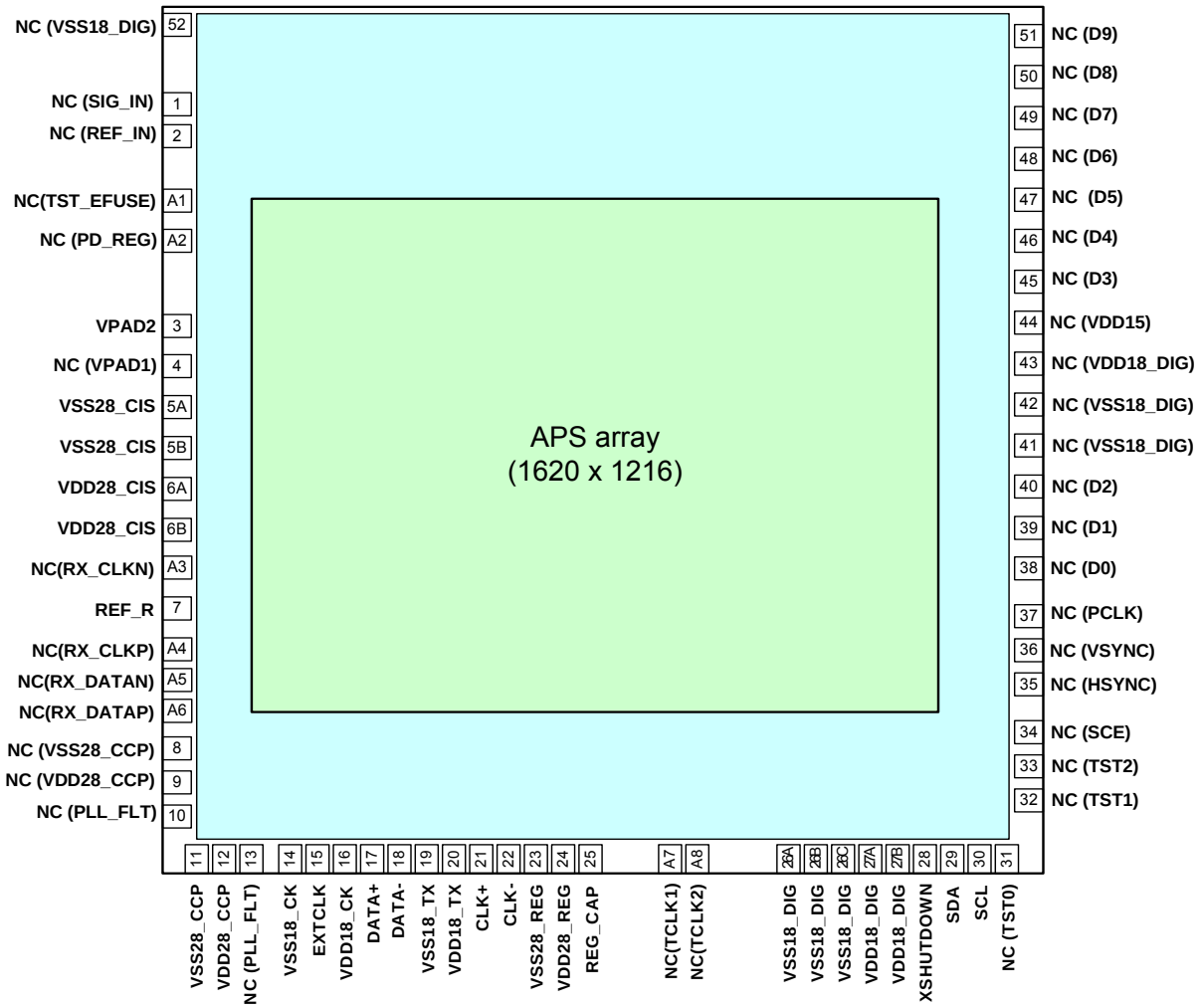


Figure 2 : Chip PAD Configuration

MODULE PIN DESCRIPTION

Table 2 : Module Pin Description

Pad No	Pad Name	Direction	Description
1	**NC**	-	No connection
2	**VCAP**	ANA	External Capacitor connected to Ground 100nF for resolutions up to SVGA 200nF for resolutions greater than SVGA VCAP Maximum Voltage = 4.2V **Capacitor Specification:** 0402 Type, X5R dielectric, K tolerance (+/-10%), Rated Voltage 10V
3	**AGND**	POWER	Analogue ground
4	**VANA**	POWER	Analogue power Local Decoupling 100nF capacitor to ground
5	**XSHUTDOWN**	IN	Active low shutdown signal
6	**EXTCLK**	IN	Input clock from host system
7	**SCL**	IN	CCI clock signal
8	**SDA**	IN/OUT	CCI data signal
9	**DGND**	POWER	Digital ground
10	**CLK-**	OUT	Differential CCP2 clock signal (negative)
11	**CLK+**	OUT	Differential CCP2 clock signal (positive)
12	**VDIG**	POWER	Digital power Local Decoupling 100nF capacitor to ground
13	**DATA-**	OUT	Differential CCP2 data signal (negative)
14	**DATA+**	OUT	Differential CCP2 data signal (positive)
15	**DGND**	POWER	Digital ground
16	**NC**	-	No connection

MODULE PIN CONFIGURATION

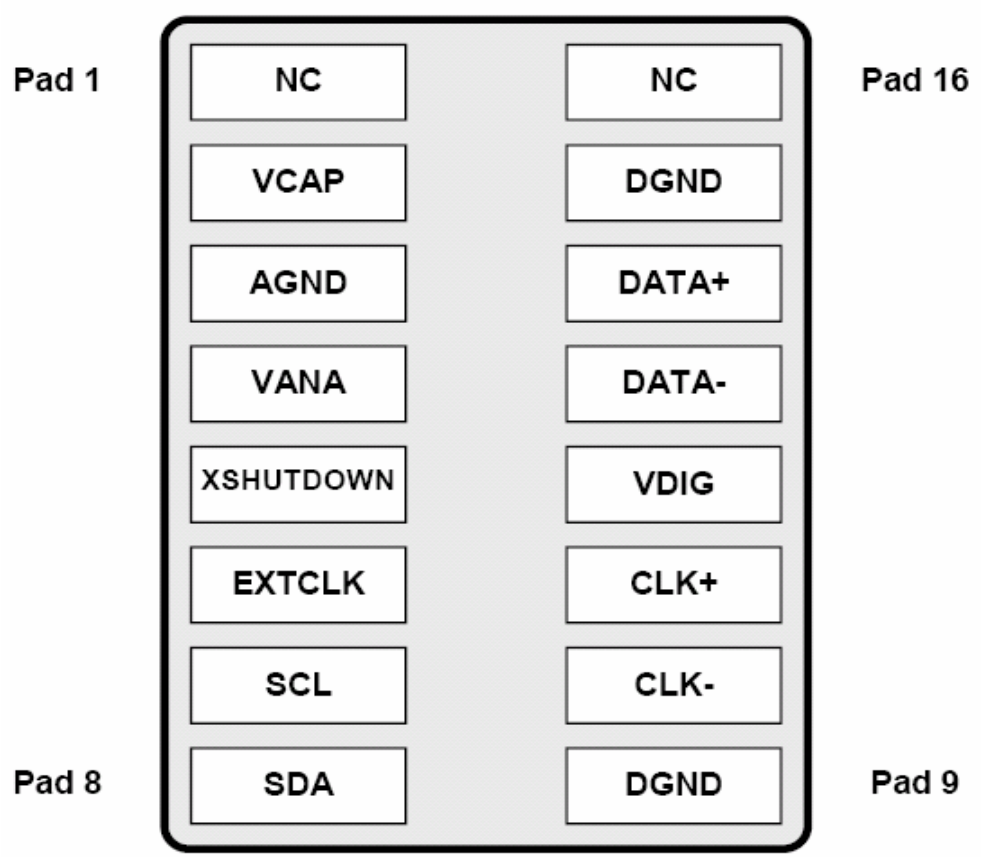


Figure 3 : Module Pin Description

PIXEL ARRAY INFORMATION

(TOP VIEW ON CHIP. DISPLAYED IMAGE WILL BE FLIPPED.)

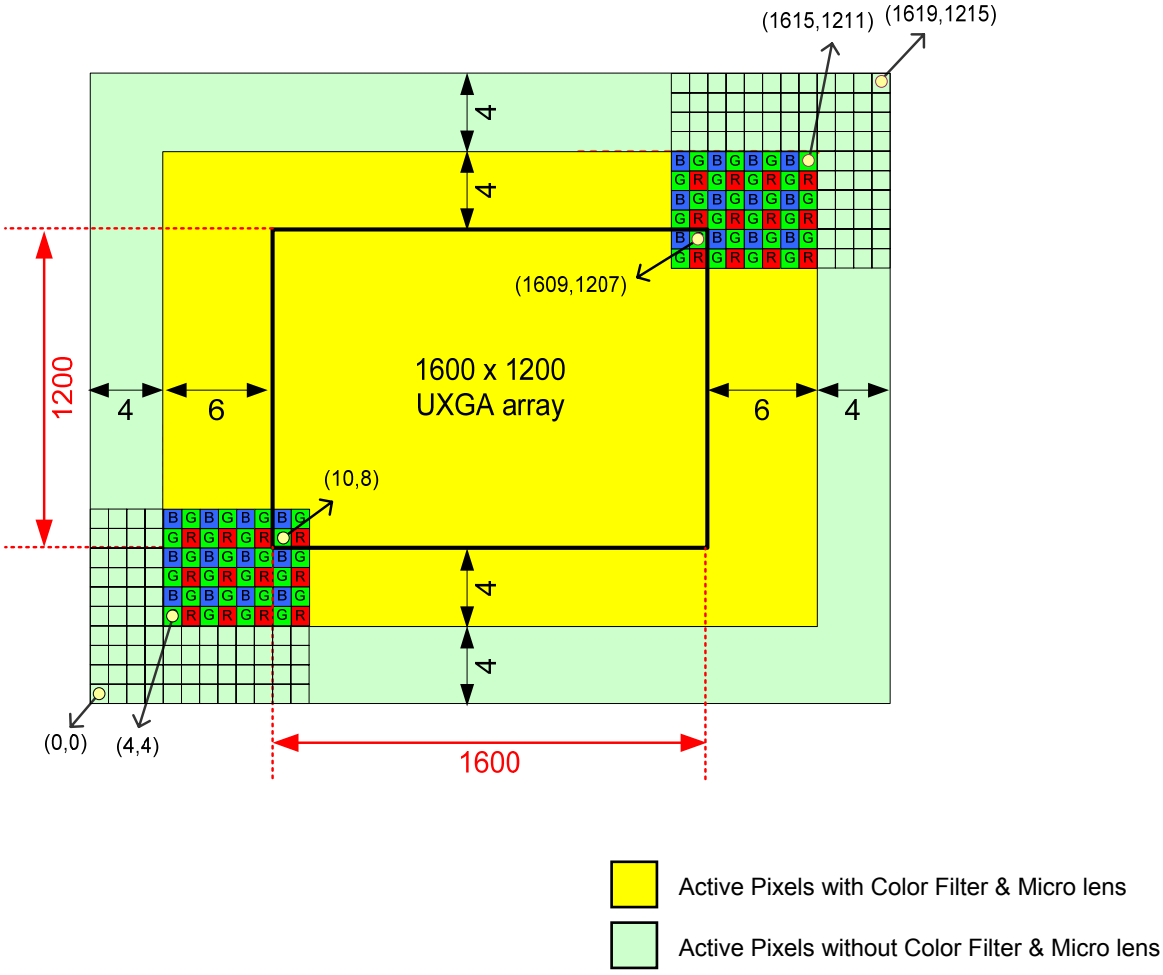


Figure 4 : Pixel Array Information

I/O TIMING DESCRIPTION

Video Output Timing

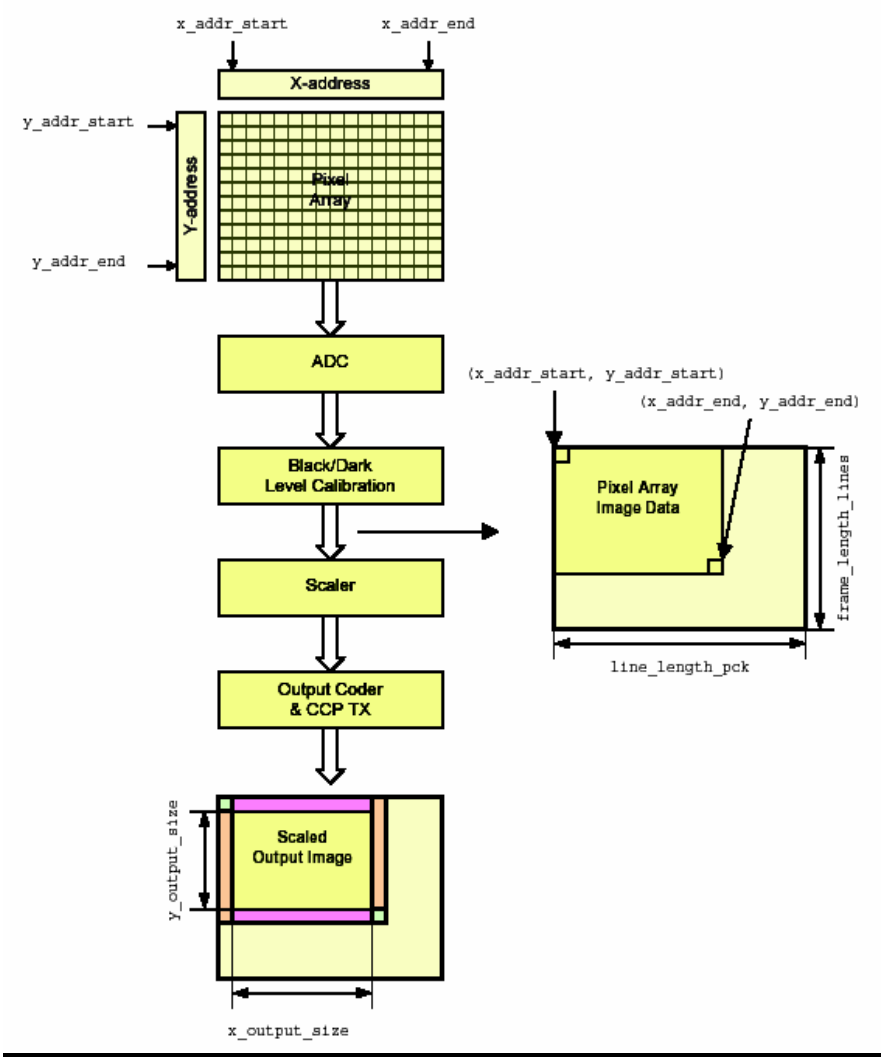


Figure 5 : Video Timing Overview

Control Interface Timing

1. Camera Control Interface (CCI)

S5K3B2FA supports the Camera Control Interface (CCI), which is an I2C Fast-mode compatible interface for controlling the transmitter. The CCP2 receiver is always a master and CCP2 transmitter always a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically no other devices than CCP2 receiver and transmitter are connected to the CCI bus. This makes a pure SW implementation possible.

Typically the CCI is separate from the system I2C bus, but I2C compatibility ensures that it is also possible to connect the transmitter to system I2C bus. CCI is a subset of I2C protocol including the minimum combination of obligatory features for I2C slave device specified in the I2C specification. Therefore transmitters complying with the CCI specification can also be connected to system I2C bus. However, it has to be taken care that the I2C masters do not try to utilize those I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conforming the CCI specification may have additional features implemented to support I2C.

1.1 Data transfer protocol

The data protocol is according to I2C standard specified in I2C specification.

1.1.1 Message format

The S5K3B2FA CCI supports 16-bit index with 8-bit data with basic I2C standard protocol; START condition, slave address with read/write bit, acknowledge from slave, and STOP condition. In read operation, data byte comes from slave till negative ack is asserted from master. The device address for the sensor is “0010_000b + 1bit R/W bit”. (Write mode : 0010_0000b, Read mode : 0010_0001b)

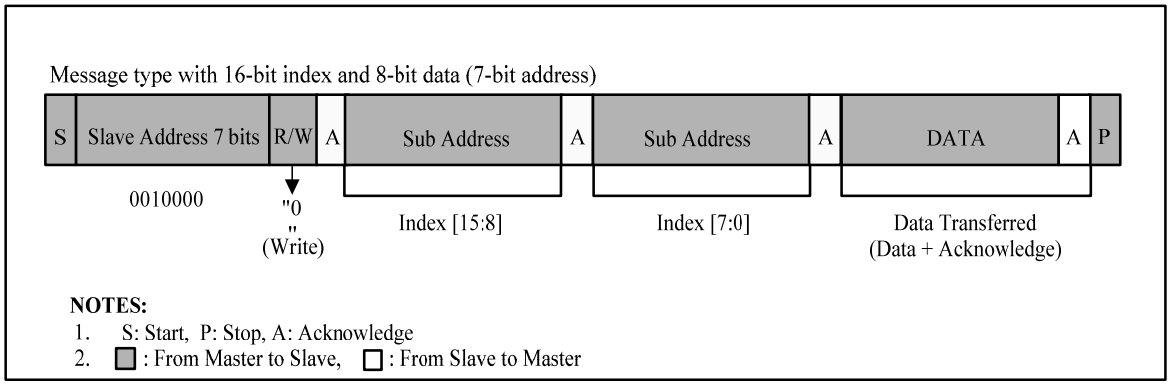


Figure 6 : CCI message type

1.1.2 Read / Write operation

The S5K3B2FA CCI interface must be able to support four different read operations and two different write operations; single read from random location, sequential read from random location, single read from current location, sequential read from current location, single write to random location and sequential write starting from random location. The read/write operations are presented in the followings. The 16bit index in the slave device has to be auto incremented after each read/write operation.

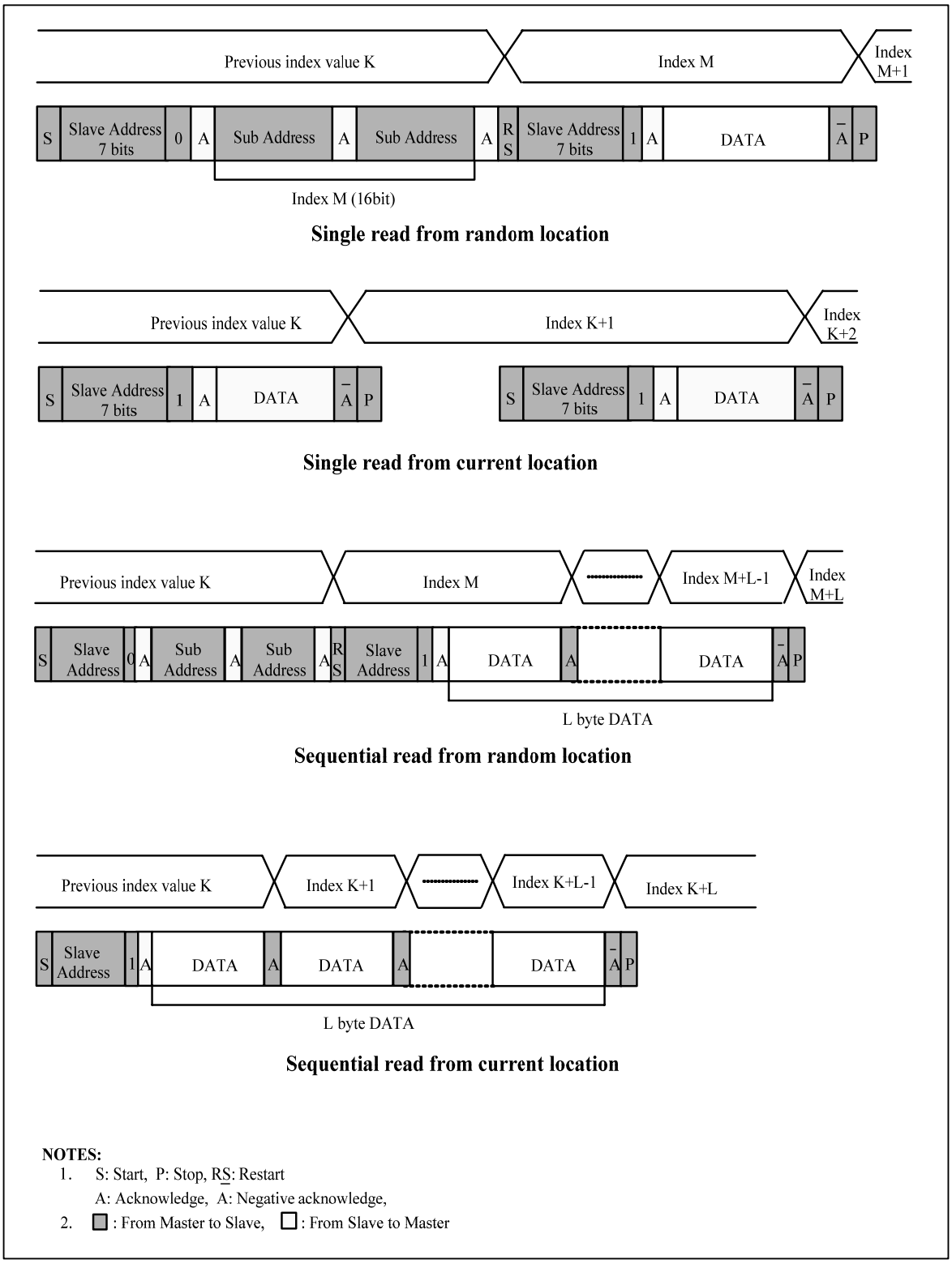
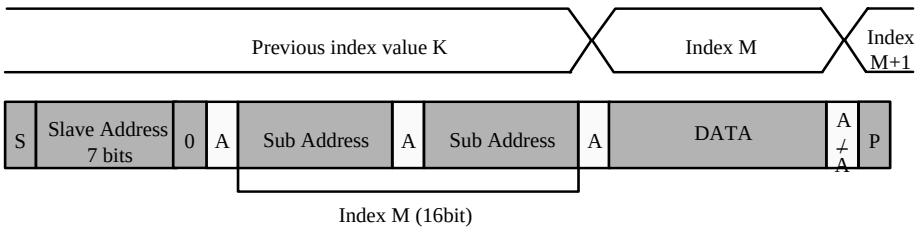
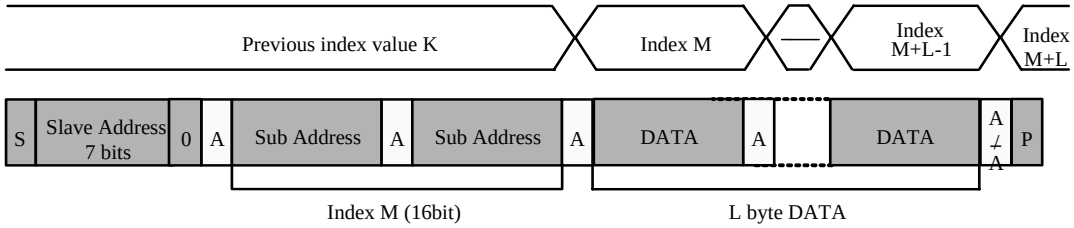


Figure 7 : CCI read operation



Single write to random location



Sequential write starting from random location

NOTES:

1. S: Start, P: Stop, RS: Restart
   A: Acknowledge, A: Negative acknowledge,
2. ■ : From Master to Slave, □ : From Slave to Master

Figure 8 : CCI write operation

FUNCTIONAL DESCRIPTION

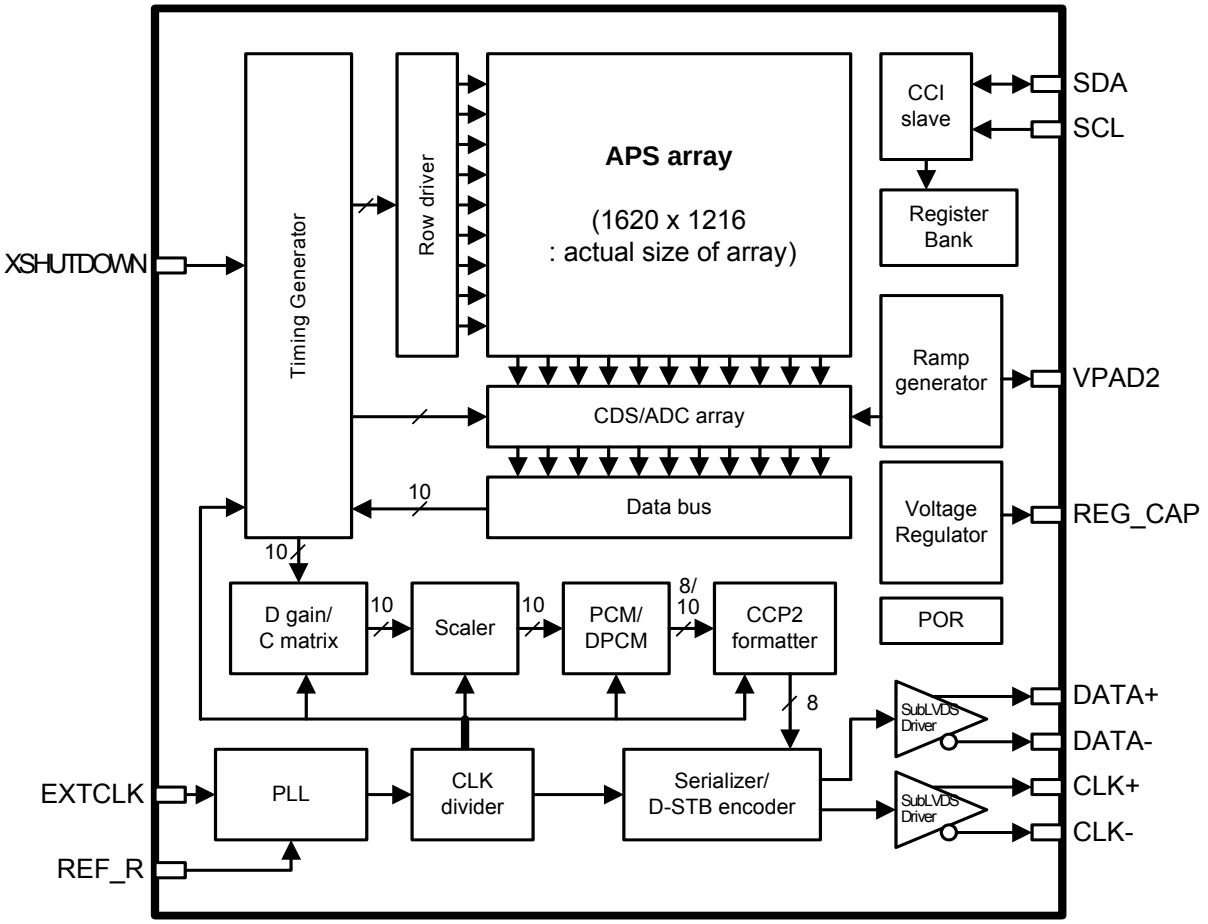


Figure 9 : Function Block Diagram

1. Output Data Format

1-1. Pixel array addresses

Addressable pixel array is defined as the pixel address range to be read. The Addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by **x_start_addr**, **y_start_addr**, **x_end_addr** and **y_end_addr** register. Figure 10 refers to a pictorial representation of the Addressable pixel array on the Physical pixel array. The limits for the above parameters are given by the **x_addr_min**, **y_addr_min**, **x_addr_max**, **y_addr_max** register.

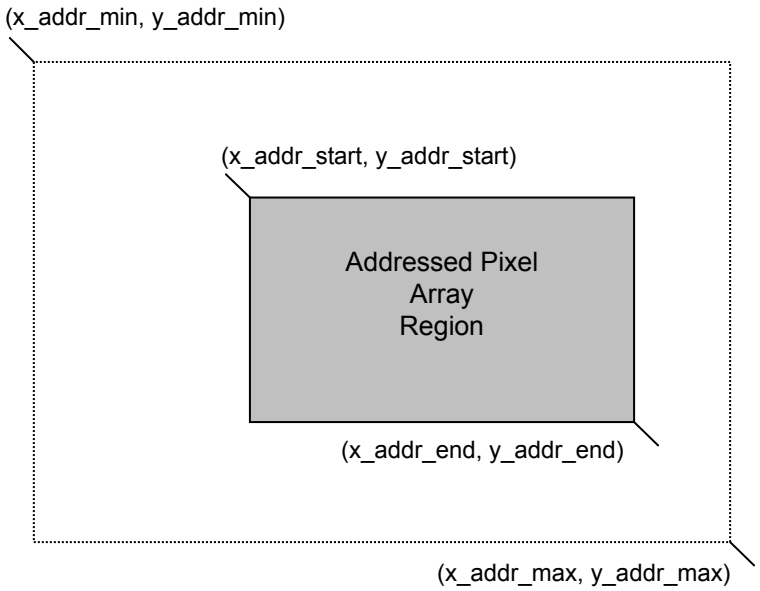
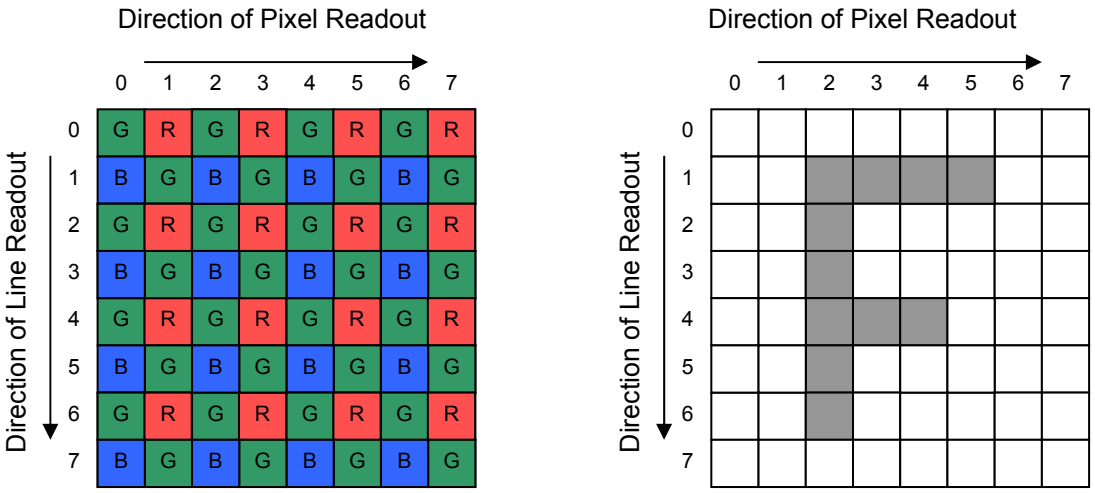


Figure 10 : Addressable Pixel Array

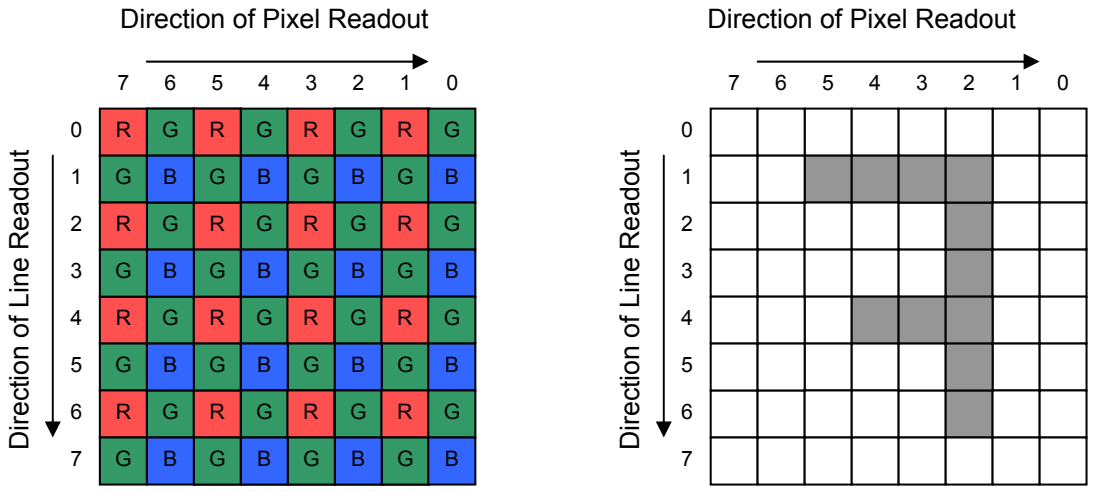
1-2. Mirror/Flip

The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror/flip mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by image orientation register.
The sensor module support 4 possible pixel readout order

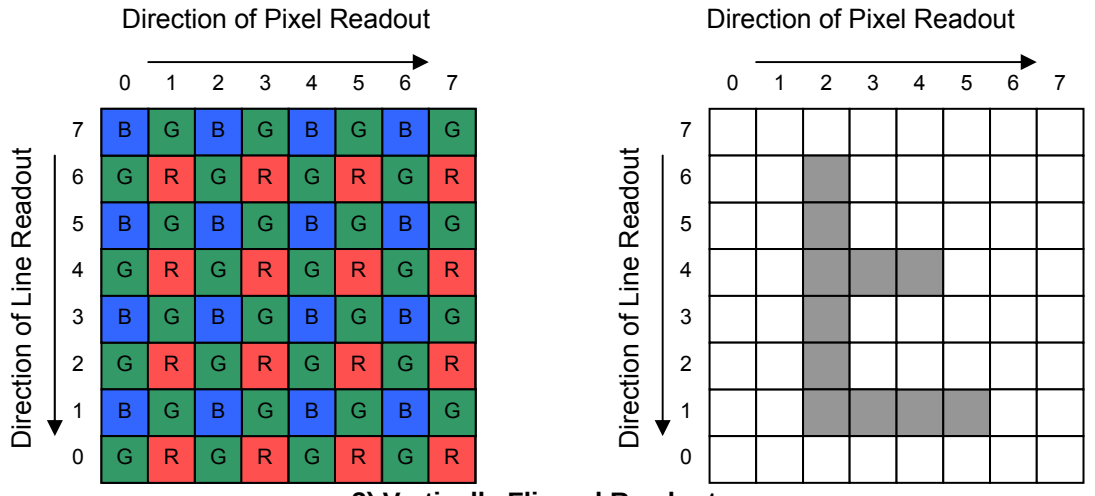
1) standard readout
2) Horizontally mirrored readout
3) Vertical Flipped readout
4) Horizontally Mirrored and Vertically Flipped readout



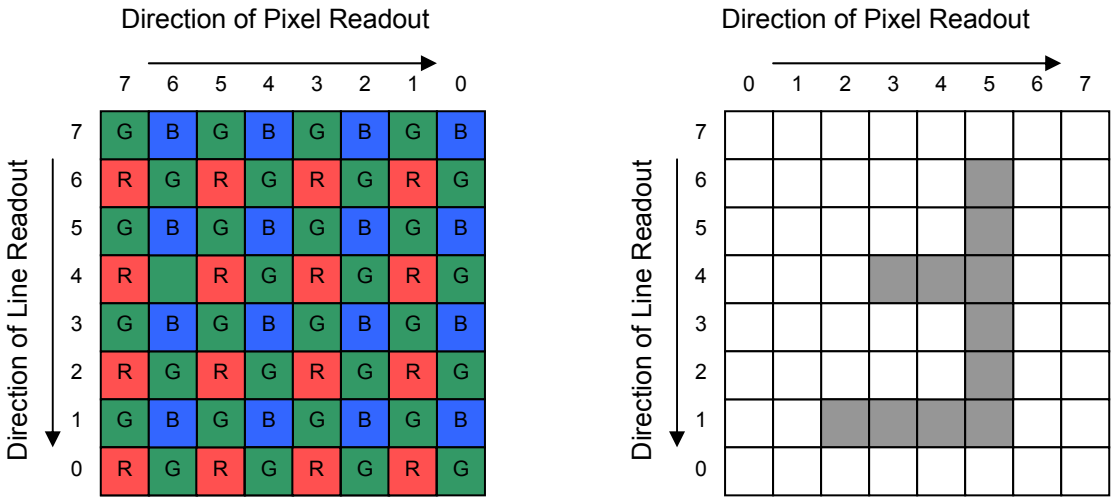
1) Standard Readout



2) Horizontally Mirrored Readout



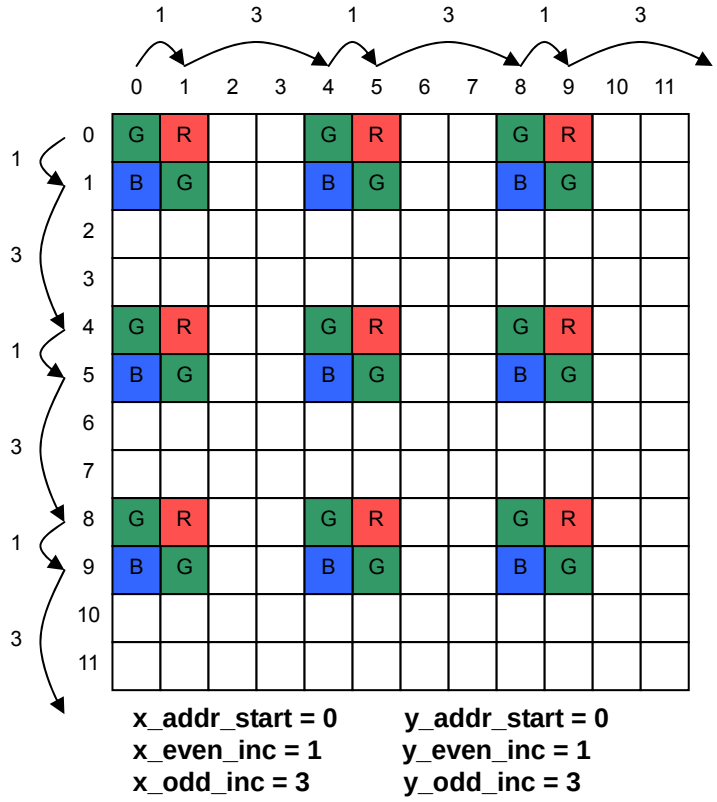
3) Vertically Flipped Readout



4) Horizontally Mirrored and Vertically Flipped Readout

1-3. Sub-Sampled readout

By programming the x and y odd and even increment register (**x_even_inc**, **x_odd_inc**, **y_even_inc**, **y_odd_inc**). the sensor can be configured to readout sub-sampled pixel data.



x_addr_start = 0
x_even_inc = 1
x_odd_inc = 3

y_addr_start = 0
y_even_inc = 1
y_odd_inc = 3

1-4. Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of virtual frame. The virtual frame's width and depth are controlled by **line_length_pck** and **frame_length_lines** register. The frame rate can be calculated by the following equation:

Frame rate = 1 / (line_length_pck * frame_length_lines) * vt_pix_clk_freq_mhz

For S5K3B2FA, the minimum **line_length_pck** is 1738(decimal) and other parameters can be set appropriately according to the above equation.

1-5. Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by shutter operation. In shutter operation, the amount of time, integration time, is determined by the column Step Integration Time Control Register (**fine_integration_time**) and line Step Integration Time Control Register(**coarse_integration_time**). The total integration time of sensor module can be calculated using the following formula.

Total_integration_time =
{(coarse_integration_time*pixel_period_per_line)+fine_integration_time}*pck_clk_period

1-6. Dark Level Compensation

The data pedestal is the pixel value the sensor module produces when there is no light incident on the sensor module. The sensor module must have an internal calibration function, which ensures that data pedestal value remains constant with integration time, gain, and temperature and between different sensors. The host system should always use the data_pedestal register value to determine the sensor output black level.

Register Name	Type	RW	Comment
data_pedestal	16-bit unsigned integer	RO Static	

System	Typical Data Pedestal
8-bit	16
10-bit	64

1-7. Image Format

Format	Bit stream	False Sync. Protection (FSP)
RAW8	P1[7:0] P2[7:0] P3[7:0] P4[7:0] P5[7:0]	P : 1~255
RAW10	P1[9:2] P2[9:2] P3[9:2] P4[9:2] P4[1:0] P3[1:0] P2[1:0] P1[1:0]	P : 4~1023, check every 5th byte

2. Analog to Digital Converter (ADC)

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

2-1. Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate those noise components, a Correlated Double Sampling(CDS) circuit is used before converting to digital. The output signal sampled twice, once for the reset level and once for the actual signal level sampling.

2-2. Analog Gain Control

The user can control the gain of pixel signal by Analog Gain Control Register (**analogue_gain_code_global**). According to SMIA 1.0 specification, the analog gain can be given by the following equation:

$$\text{Analog Gain} = (m_0 \times + c_0) / (m_1 \times + c_1)$$

S5K3B2FA specifies analog gain by coefficients of $m_0 = 0$, $c_0 = 128$, $m_1 = -1$, $c_1 = 128$. As a result, users can control analog gain as following equation:

$$\text{Analog Gain} = 128 / (128 - \textbf{analogue\_gain\_code\_global}[15:0])$$

Separate channel gain is also supported in addition to global analog gain. Theoretically, maximum x128 gain can be obtained, but analog gain up to x8 is recommended for image quality.
The Maximum error in analog gain is as follows:

Analog Gain = 2x (**analogue_gain_code_global**[15:0]=0x0040) ➔ +/- 10%
Analog Gain = 8x (**analogue_gain_code_global**[15:0]=0x0070) ➔ +/- 30%

Under all conditions, increasing analogue gain always gives an increase in the applied analogue gain and output code.

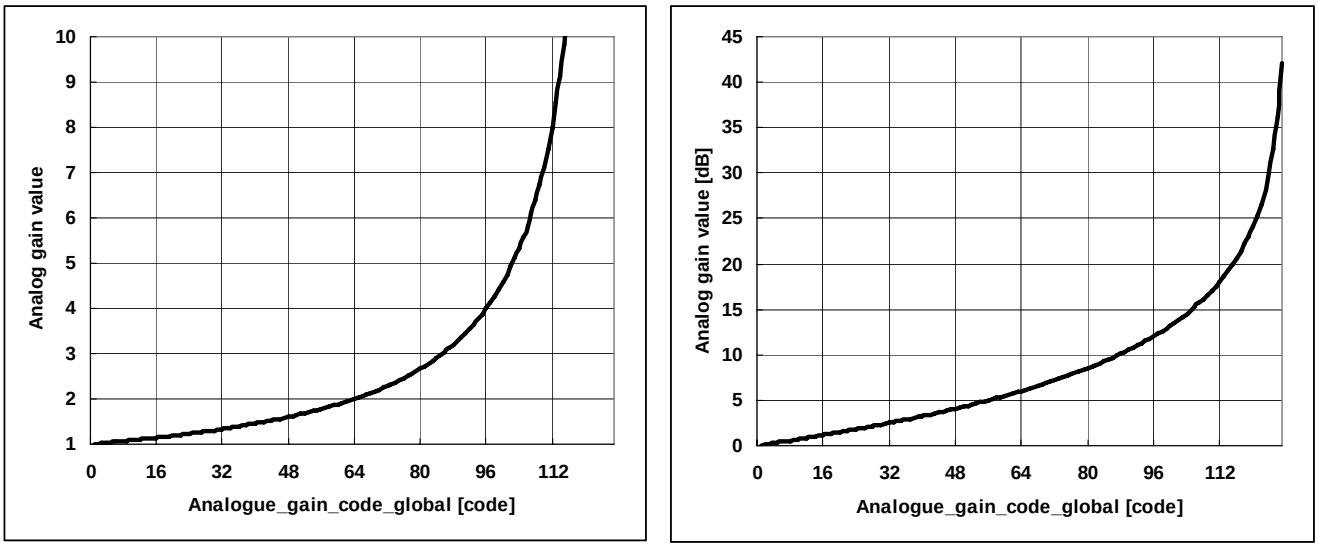


Figure 11 : Analog Gain Value

3. Image Scaling and Data Interface

The S5K3B2FA is a high performance and low power UXGA CMOS image sensor with image scaling functions. It generates 10-bit raw data from 10-bit sensor with maximum frame rate of 30 fps at UXGA resolution and transmits the data in the forms of RAW10, RAW8 specified in SMIA CCP2 Specification 1.0.
It performs image scaling functions for horizontal/full scaling. The host controller is able to access and control it through CCI bus interface (also specified in SMIA CCP2 Specification 1.0).

3-1. PLL and Clock Generator

S5K3B2FA contains a Phase-Locked Loop(PLL) and a clock generator, which generates all the necessary video timing and output pixel clocks from the external clock input. By setting the divide-ratio for Pre PLL Clock Divider(**pre_pll_clk_div**) and PLL Multiplier(**pll_multiplier**) appropriately, users can get necessary PLL output Clock(**pll_op_clk_freq_mhz**). The minimum and maximum limits for the output clock frequencies and divide-ratios of the various clock dividers are fully described and limited by the Parameter Limit Registers (Read Only) from 0x1100 to 0x1177 address. The PLL can handle any **ext_clk_freq_mhz** in the range of 6.0MHz to 27MHz, and synthesize **pll_op_clk_freq_mhz** between 324MHz and 650MHz by **2 steps of pll_multiplier**. For the proper PLL operation, **pll_ip_clk_freq_mhz** should be in the range of 1MHz to 6MHz. All PLL programming should be performed during software stand-by mode for the stable system operation.

The overall clock tree structure is shown in Figure 12, and there are user-controllable divide-ratios in the red box. All necessary frequencies are synthesized by the following equations.

pll_ip_clk_freq_mhz = ext_clk_freq_mhz / pre_pll_clk_div **(pll_ip_clk_freq_mhz : 1MHz ~ 6MHz)**
pll_op_clk_freq_mhz = pll_ip_clk_freq_mhz * pll_multiplier **(pll_op_clk_freq_mhz : 324MHz ~ 650MHz)**
vt_sys_clk_freq_mhz = pll_op_clk_freq_mhz / vt_sys_clk_div
vt_pix_clk_freq_mhz = pll_op_clk_freq_mhz / (vt_sys_clk_div * vt_pix_clk_div)
op_sys_clk_freq_mhz = pll_op_clk_freq_mhz / op_sys_clk_div
op_pix_clk_freq_mhz = pll_op_clk_freq_mhz / (op_sys_clk_div * op_pix_clk_div)

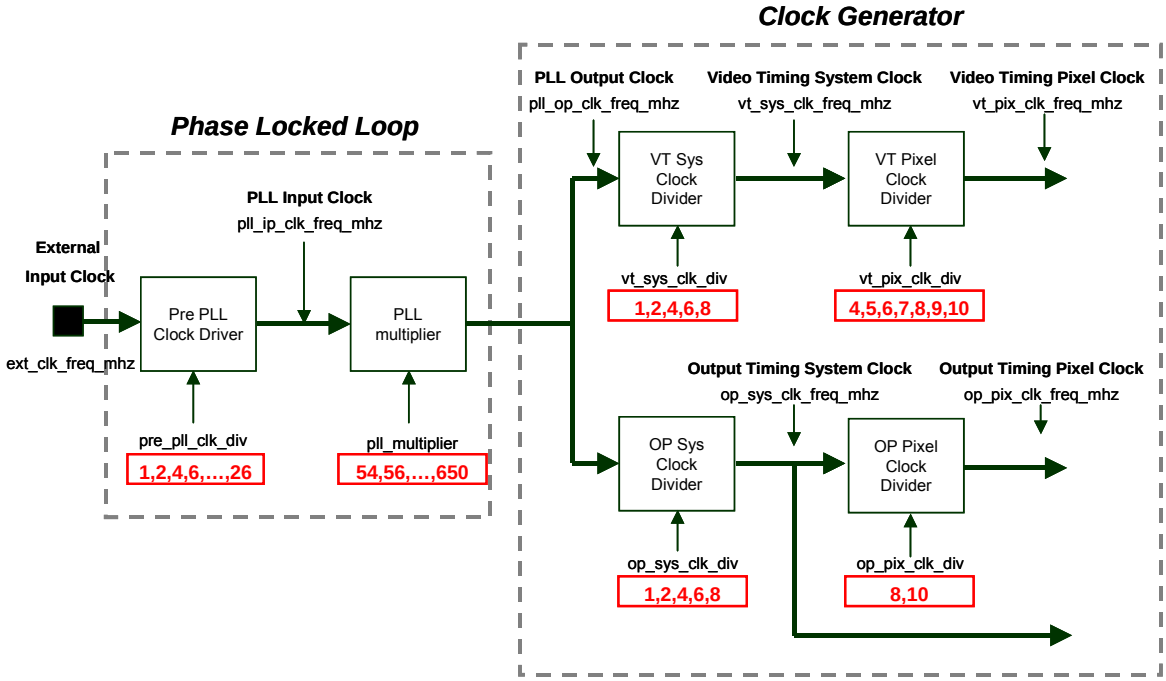


Figure 12 : Clock tree structure

3-2. Scaler

The image scaling function within the sensor module provides a flexible way of generating lower resolution full field of view image data, at a reduced data rates, for viewfinder and video applications. The scaler is able to scale the full resolution of the sensor module down to within 10% of a the target image size (the smallest output size is 256x192). This flexibility means that sensor modules can support a wide range of LCD viewfinder sizes and different codec resolutions

To provide a wider range of data rate reduction options the full image scaler is able to reduce the data rates in both the horizontal and vertical directions. This is achieved by the use of a FIFO between video timing and output clock domains (Figure 13).

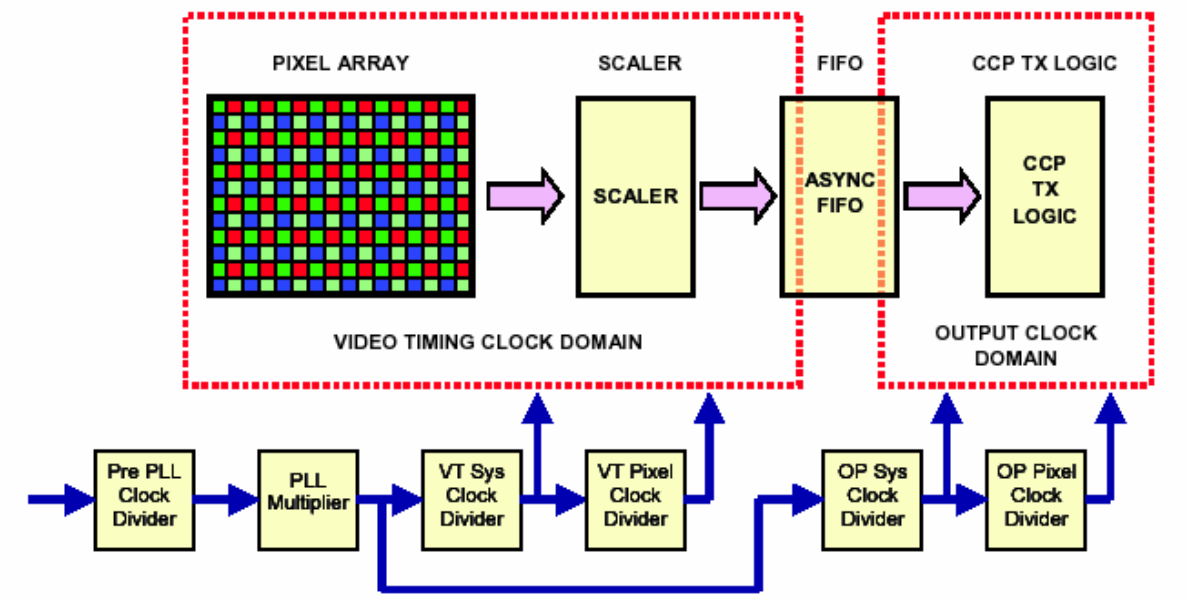


Figure 13 : Full Scaler Block Diagram

Clock divider setting restrictions are as follows when scaling mode is on:

$$1 \le \frac{op\_sys\_clk\_div \times op\_pix\_clk\_div}{vt\_sys\_clk\_div \times vt\_pix\_clk\_div} \le \left(\frac{scale\_m}{scale\_n}\right)^2 \quad \text{, for full scale down}$$

$$1 \le \frac{op\_sys\_clk\_div \times op\_pix\_clk\_div}{vt\_sys\_clk\_div \times vt\_pix\_clk\_div} \le \left(\frac{scale\_m}{scale\_n}\right) \quad \text{, for horizontal scaling only}$$

For the proper scaler operation, the **fifo_water_mark_pixels** register value should be specified according to the scale_m as described below :

fifo_water_mark_pixels = the horizontal width of visible pixels / scale-down factor + 10
where scale-down factor = scale_m / scale_n and decimal 10 is the marginal value for safe operation.

For example, when 'the horizontal width of visible pixels is 1608 and scale_m is 20', fifo_water_mark_pixels becomes 1296 (1608 / (20/16) + 10 ≈ 1296).

3-3. CCP2 Frame Format

The frame format is specified by Frame Descriptors. There are 3 descriptors in S5K3B2FA, one for column, two for row. Each describes the visible column width, embedded data lines, visible row width. Figure 14 shows our default Frame Descriptor value.

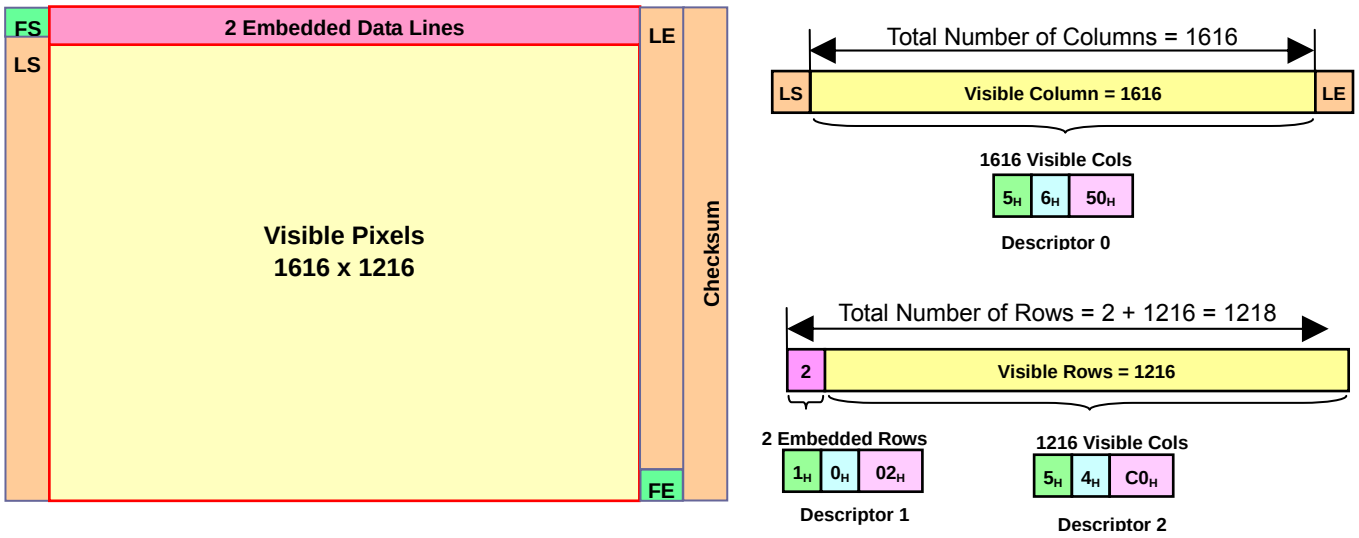


Figure 14 : Frame Format

3-4. Test Pattern

Two types of full frame deterministic test patterns are defined. Most are Bayer test patterns more suitable for some tests than real image data and are injected early in the sensor data path. The only exception to this is a test pattern that is intended to test sensor-host link integrity, the data in this pattern is not Bayer data and it is injected just prior to CCP2 framing.

Use of these full frame test patterns is controlled by the test_pattern_mode parameter. The following table shows all the defined parameter settings.

Parameter Name	Type	R/W	Coding	Function
test_pattern_mode	16-bit unsigned integer	RW	0 – no pattern (default) 1 – solid color 2 – 100 % color bars 3 – fade to grey color bars 4 – PN9 (no embedded lines) 5 – 255 reserved 256-65535 – manufacturer specific	Controls the output of the test pattern mode

3-5. PN9 Code Generation

The PN9 test pattern is included to ease testing of sensor-link integrity (measurement of bit error rate etc). PN9 linear feedback shift register has the polynomial X^9+X^5+1 in Fibonacci type notation (Figure 15). The reset value of PN9 is 0x1FF.

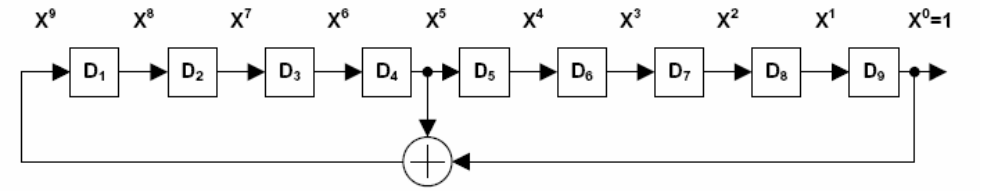


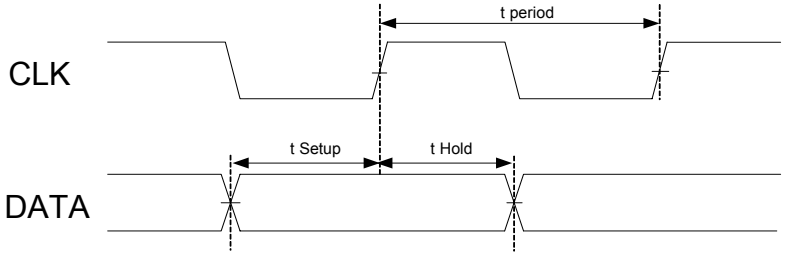
Figure 15 : PN9 Linear Feedback Shift Registers

3-6. CCP2 and SubLVDS

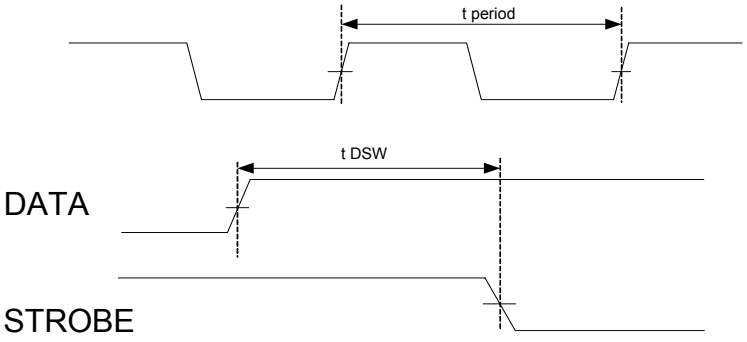
The CCP2 specification defines standard data transmission and control interfaces between transmitter and receiver. Data transmission interface (referred as CCP2) is unidirectional differential serial interface with data and clock/strobe signals.
CCP2 defines two options for data transfer between transmitter and receiver. The first one is normal data and clock. The second one is based on signaling scheme called data-strobe, which is a method for data transfer not needing a continuous clock signal. The clock is reconstructed at the receiving end from the data and strobe signals. The physical layer of CCP2 is based on signaling scheme called SubLVDS, which is current mode differential low voltage signaling method modified from the IEEE 1596.3 LVDS standard for reduced power consumption. Electrical specifications for the SubLVDS I/O's can be found from chapter 9, SMIA1.0 Part 2: CCP2 specification. The use of data-strobe coding together with SubLVDS enables the use of high data rates with low EMI.
CCP2 is classified in 3 classes according to the data rate and signaling method. This sensor complies with CCP2 Class 2 (up to 650Mbps, Data/Strobe mode).

Maximum frame rates at raw 10 mode is

1600 X 1200	30 fps @ 650 Mbps data /strobe
800 X 600	60 fps @ 650 Mbps data /strobe
400 X 300	60 fps @ 650 Mbps data /strobe



t Setup(MIN) = **t** period /2 – 0.05* **t** period
t Hold(MIN) = **t** period /2 – 0.05* **t** period



0.98* **t** period < **t** DSW < 1.02* **t** period

Figure 16 : CCP Timing Specifications

POWER UP SEQUENCE

The digital and analogue supply voltages can be powered up in any order e.g. VDIG then VANA or VANA then VDIG.
On power up :

- If XSHUTDOWN is low when the power supplies are brought up then the sensor module will go into hardware standby mode.
- If XSHUTDOWN is high when the power supplies are brought up then the sensor module will go into software standby mode

In both cases the presence of an on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values. The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

Table 3 : Power-Up Sequence Timing Constraints

Constant	Label	Min	Max	Units
VANA rising – VDIG rising	t0	VANA and VDIG may rise in any order. The rising separation can vary from 0ns to indefinite		ns
VDIG rising – VANA rising	t1			ns
VANA rising – XSHUTDOWN rising	t2	0.0	-	ns
XSHUTDOWN rising – First I2C transaction	t3	2400	-	EXTCLK cycles
Minimum No. of EXTCLK cycles prior to the first I2C transaction	t4	2400	-	EXTCLK cycles
PLL start up/lock time	t5	-	1	ms
Entering streaming mode – first frame start sequence (fixed part)	t6	-	10	ms
Entering streaming mode – first frame start sequence (variable part)	t7	The delay is the coarse integration time value		lines

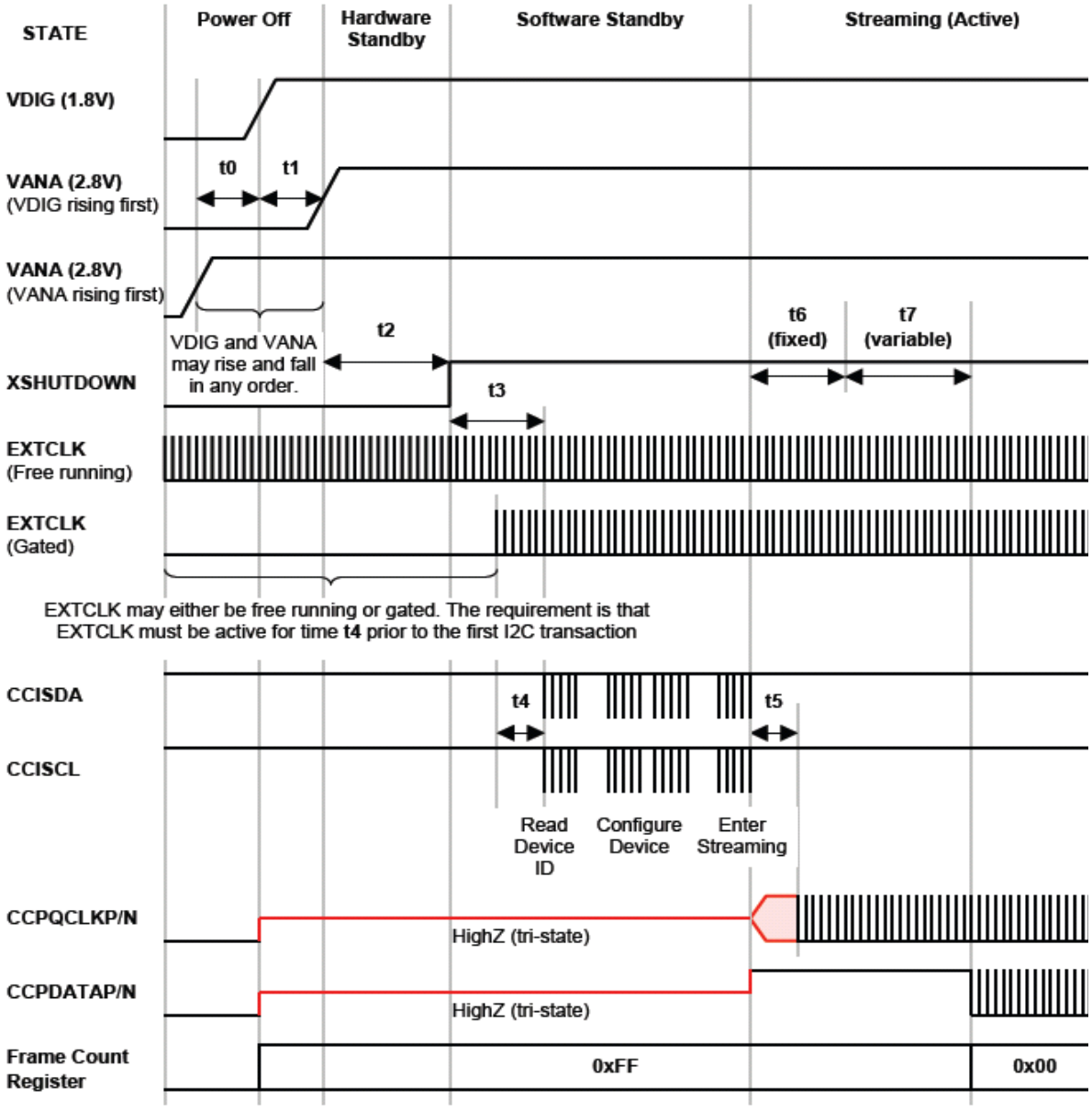


Figure 17 : Power-Up Sequence

POWER DOWN SEQUENCE

The digital and analogue supply voltages can be powered down in any order e.g. VDIG then VANA or VANA then VDIG.
Similarly to the power-up sequence the EXTCLK: input clock may be either gated or continuous.

If the CCI command to exit streaming is received while a frame of CCP2 data is being output then the sensor module must wait to the CCP2 frame end code before entering software standby mode.

If the CCI command to exit streaming mode is received during the inter frame time then the sensor module must enter software standby mode immediately.

Table 4 : Power-Down Sequence Timing Constraints

Constant	Label	Min	Max	Units
Enter Software Standby CCI command – Device in Software Standby mode	t0	If outputting a frame of CCP2 data waits to CCP2 frame end code before entering software standby, otherwise enter software standby mode immediately.		
Minimum no of EXTCLK cycles after the last I^2C transaction or CCP2 frame end	t1	512	-	EXTCLK cycles
Last I^2C Transaction or CCP2 frame end – XSHUTDOWN falling	t2	512	-	EXTCLK cycles
XSHUTDOWN falling – VANA falling	t3	0.0	-	ns
VANA falling – VDIG falling	t4	VANA and VDIG may fall in any order. The falling separation can vary from 0ns to Indefinite.		ns
VDIG falling - VANA falling	t5			ns

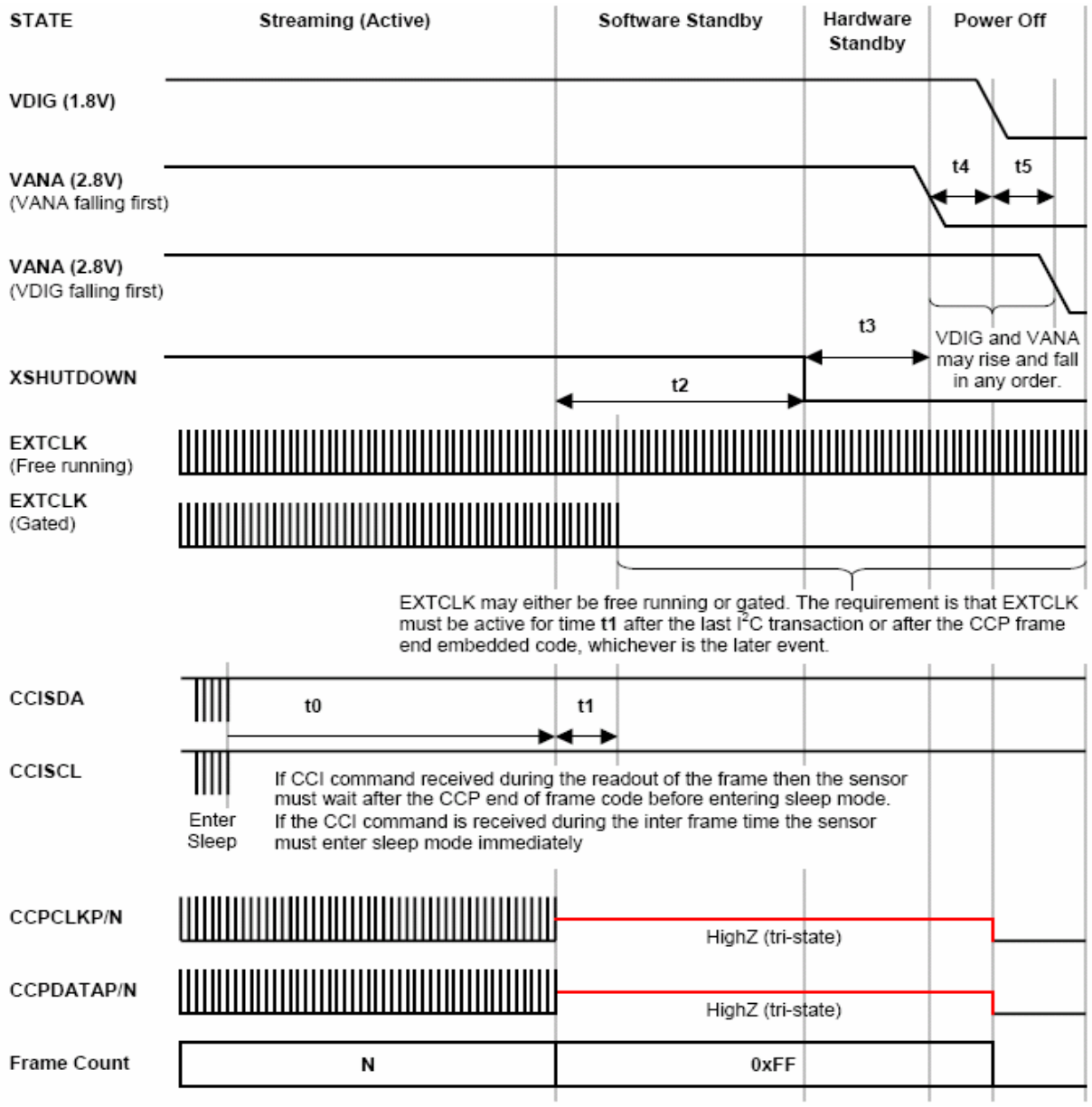


Figure 18 : Power-Down Sequence

INTERNAL POWER-ON RESET

The sensor module should internally perform a power-on reset (POR) when the digital supply rises above a trigger level, V_{trig_rising}.
Similarly is the digital power supply falls below the trigger level, $V_{trig\_falling}$, then the power-on reset should activate.
The host must be able to reset the sensor by turning the power supplies on and off.

Table 5 : Internal Power-on Reset Cell Specifications

Constraint	Label	Min	Typ	Max	Units
VDIG rising crossing V_{trig_rising} – Internal reset being released	t1	7	10	15	us
VDIG falling crossing $V_{trig\_falling}$ – Internal reset active	t2	-	0.5	1	us
Minimum VDIG spike width below $V_{trig\_falling}$ which is considered to be a reset when POR cell output high	t3	0.4	0.5	-	us
Minimum VDIG spike width below $V_{trig\_falling}$ which is considered to be a reset when POR cell output low	t4	0.5	1.0	-	us
Minimum VDIG spike width above V_{trig_rising} which is considered to be a supply is stable when POR cell output low. While the POR cell output is low all VDIG spikes above V_{trig_rising} that are less than t5 must be ignored.	t5	-	50	-	ns
VDIG rising trigger voltage	V_{trig_rising}	1.15	1.4	1.55	V
VDIG falling trigger voltage	$V_{trig\_falling}$	1.00	1.25	1.45	V

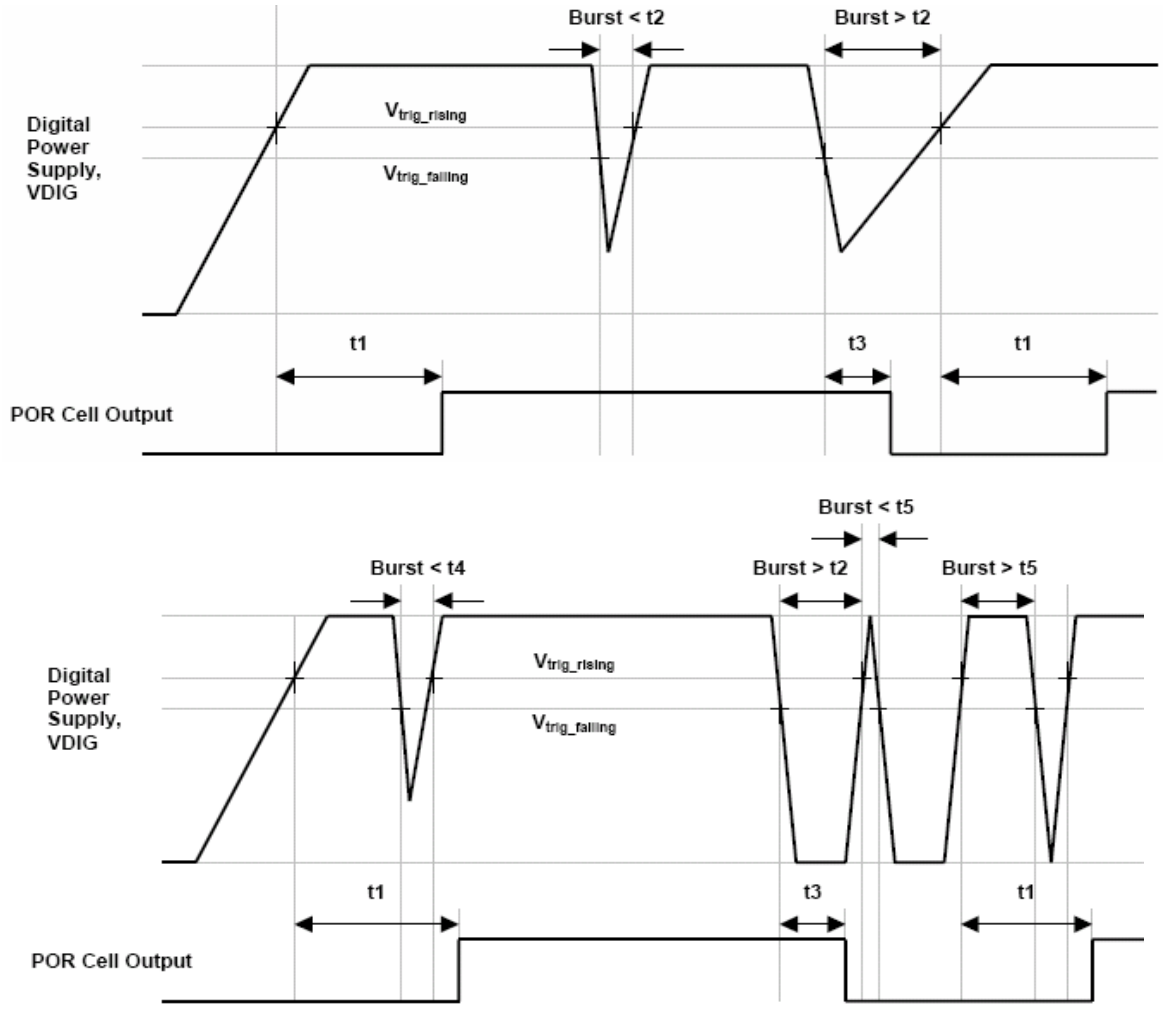


Figure 19 : Power-on Reset Power-up and Supply Glitch/Brown-out Timing

STAND-BY SEQUENCE

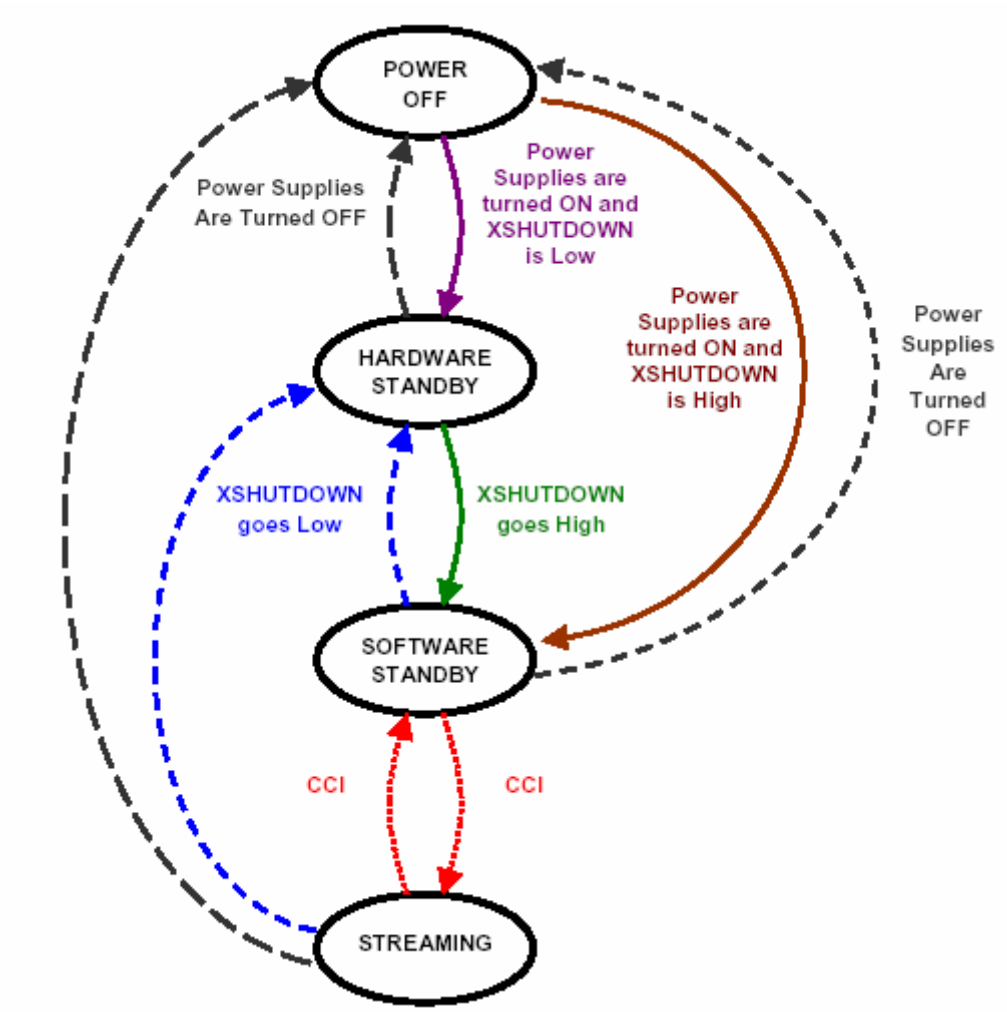


Figure 20 : Stand-By Sequence

ELECTRICAL CHARACTERISTICS

Table 6 : Absolute Maximum Rating

Symbol	Description	Min	Typical	Max	Units
$V_{DIG(MAX)}$	Digital Absolute Max (1)	-0.3	-	2.2	V
$V_{ANA(MAX)}$	Analogue Absolute Max (2)	-0.3	-	4	V
$V_{IP(DIG)}$	Digital Input Voltages (3)	-0.3	-	V_{ANA}+0.3	V
VCAP	VCAP Analogue Voltage	-0.3	-	4.2	V
T_{STR}	Storage Temperature	-40	-	85	°C

[Notes:]
(1) Digital Supply 1.9V + 0.3V
(2) Analogue Supply 2.9V + 1.1V
(3) Digital Inputs: EXTCLK, XSHUTDOWN, SCL, SDA

Table 7 : Operating Conditions

Symbol	Description	Min	Typical	Max	Units
V_{DIG}	Digital Absolute Max (1)	1.7	1.8	1.9	V
V_{ANA}	Analogue Absolute Max (2)	2.4	2.8	2.9	V
$V_{IP(DIG)}$	Digital Input Voltages (3)	0	-	V_{ANA}	V
VCAP	VCAP Analogue Voltage	0	-	4.2	V
T_{TEST}	Test Temperature (4)	21	23	25	°C
T_{OPT}	Optimum Operating Temperature (5)	5	-	40	°C
T_{OPR}	Normal Operating Temperature (6)	-25	-	55	°C
T_{FUNC}	Functional Operating Temperature (7)	-30	-	70	°C

[Notes:]
(1) Digital Supply tolerances: 1V8 +/- 100mV
(2) Analogue Supply Tolerances: Lower limit 2V5-100mV, Upper Limit: 2V8+100mV
(3) Digital Inputs: EXTCLK, XSHUTDOWN, SCL, SDA
(4) Test Temperature – image quality test conditions
(5) Optimum Operating Temperature – no visible degradation in image quality
(6) Normal Operating Temperature – camera produces acceptable images
(7) Functional Operating Temperature – camera fully functional

Table 8 : DC Characteristics

(V_{ANA} = 2.4V ~ 2.9V, V_{DIG} = 1.8V ± 0.15V, Ta = -30 to +70 °C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Input voltage(1)	V_{IH}	-	0.7*V_{DIG}	-	-	V
	V_{IL}	-	-	-	0.3*V_{DIG}	
Input leakage current(1)	I_{IL}	V_{IN} = V_{ANA} to DGND	-10	-	10	uA
High level output voltage (2)	V_{OH}	I_{OH} = -4mA	V_{DIG}-0.2	-	-	V
Low level output voltage (2)	V_{OL}	I_{OL} = 4mA	-	-	0.2*V_{DIG}	
High-Z output leakage current (3)	I_{OZ}	V_{OUT} = V_{SS} or V_{DIG}	-10	-	10	uA
Input capacitance(1)	C_{IN}	-	-	-	4	pF
Differential voltage swing (4)	V_{OD}	Termination resistor=100Ω	100	150	200	mV
Fixed common mode voltage (4)	V_{CMF}	-	0.8	0.9	1.0	V
Drive current range (4)	I_{DRV}	Termination resistor=100Ω	0.833	1.5	2	mA
Drive current variation (4)	D_{IO}	-	-	-	15	%
Output impedance (4)	R_O	-	40	-	140	Ω
Output impedance mismatch (4)	D_{RO}	-	-	-	10	%
Supply current (5)	I_{HWSBA}	Hardware standby mode Analog (6)	-	1.2	5	uA
	I_{HWSBD}	Hardware standby mode Digital (6)	-	4.3	15	uA
	I_{SWSB1A}	Software standby mode Analog(7)	-	39	50	uA
	I_{SWSB1D}	Software standby mode Digital(7)	-	24	50	uA
	I_{SWSB2A}	Software standby mode Analog (8)	-	39	50	uA
	I_{SWSB2D}	Software standby mode Digital (8)	-	299	500	uA
	I_{STRMA}	Streaming mode Analog (9) @ 30 fps	-	27	40	mA
		Streaming mode Analog (10) @ 15fps	-	25	38	mA

	I_{STRMD1}	Streaming mode Digital (9) (scaling off) @ 30 fps	-	35	45	mA
		Streaming mode Digital (10) (scaling off) @ 15 fps	-	22	32	mA
	I_{STRMD2}	Streaming mode Digital (9) (scale_m =32) @ 30 fps	-	33	68	mA
		Streaming mode Digital (10) (scale_m =32) @ 15 fps	-	24	55	mA

[NOTE]
(1) Applied to EXTCLK, XSHUTDOWN, SCL, SDA pins
(2) Applied to SCL, SDA pins
(3) Applied to SCL, SDA pins when in High-Z output state
(4) Applied to DATA+/DATA-, CLK+/CLK- pins
(5) Summation of currents from V_{DIG} and V_{ANA}
(6) At 25deg., External clock active or not switching
(7) External clock not switching
(8) External clock active (6MHz)
(9) Readout of the full raw Bayer image at the maximum frame rate(30fps).
(10) Readout of the full raw Bayer image at the 15fps

Table 9 : AC Characteristics

(V_{ANA} = 2.4V ~ 2.9V, V_{DIG} = 1.8V ± 0.15V, Ta = -30 to +70 °C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
External clock frequency (1) (DC-coupled)	$f_{XCLK,DC}$	-	6.0	-	27.0	MHz
External clock frequency (1) (AC-coupled)	$f_{XCLK,AC}$	-	6.0	-	27.0	MHz
External clock duty cycle (1)	f_{XDUTY}	-	45	-	55	%
EXTCLK input voltage (1) (DC-coupled)	$V_{IH,XDC}$	-	$0.7*V_{DIG}$	1.8	2.9	V
	$V_{IL,XDC}$	-	-	-	$0.3*V_{DIG}$	
EXTCLK input voltage (1) (AC-coupled)	$V_{I,XAC}$	-	0.5	1.0	1.2	Vp-p
PLL locking time	t_{LOCK}	-	-	50	-	us
Random jitter (2)	t_{RJIT}	0101 pattern at 650Mbps	-	65	-	ps(p-p)
Total jitter (3)	t_{TJIT}	PN9 pattern at 650Mbps	-	125	-	ps(p-p)
Complementary skew (4)	$t_{cmpskew}$	Within differential pair	-	-	50	ps
Channel-to-channel skew (4)	$t_{chcskew}$	Between 2-channels	-	-	100	ps
V_{OD} rise time 20%-80% (4)	t_{RISE}	20%~80% at V_{OD}	300	-	400	ps
V_{OD} fall time 80%-20% (4)	t_{FALL}	80%~20% at V_{OD}	300	-	400	ps
CCP2 Operating frequency	f_{OPR}	-	1	-	416	MHz
Power-up/down time (5)	t_{PD}	-	-	-	20	us
Power supply rejection ratio 0-100MHz (6)	PSRRL	0~100MHz	30	-	-	dB
Power supply rejection ratio 100-1000MHz (6)	PSRRH	100~1000MHz	10	-	-	dB

[NOTE]
(1) Applied to EXTCLK pin.
(2) Jitter generated by PLL only
(3) Total Jitter generated by PLL, serializer, and SubLVDS driver
(4) Applied to DATA+/DATA-, CLK+/CLK- pins
(5) Power-up and down time which SubLVDS driver fully operates and goes into Hi-Z state respectively
(6) Nominal value for the interference at V_{CM} voltage through digital supply relative to the interference at digital supply over the 0-1GHz operating range. PSRR=20*log10($V_{DDinterference}$(peak-to-peak)/$V_{CMinterference}$(peak-to-peak)

Table 10 : Electrostatic Characteristics

Index	Electrostatic Standard			UNIT	Remark
	PIN No.	Design Target	Reference Product		
Human Body Model	ALL	2000	2000	V	JESD22-A114-B
Machine Model	ALL	200	250	V	JESD22-A115-A
CDM	ALL	500	1000	V	JESD22-C101C
Latch-up	I-test	Positive trigger : Inorm+100mA Negative trigger : -100mA	-	mA	JESD78
	V supply over-voltage test	VANA,max x 1.5 & VDIG,max x 1.5	-	V	

Table 11 : CCI Timing Specifications

(V_{IHmin} = 0.9 V_{DD}, V_{ILmax} = 0.1 V_{DD}, External pull-up resister = 4.7kOhm at SCL/SDA for Fast-mode, V_{ANA} = 2.4V ~ 2.9V, V_{DIG} = 1.7V ~ 1.9V, Ta = -30 to +70 °C)

Characteristic	Symbol	Condition	Min	Typ	Max	Units
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	C_B : from 10pF to 400pF	20 + 0.1 C_B (1)	-	250	ns
Pulse width of spikes which must be suppressed by the input filter.	t_{SP}		0	-	50	ns
SCL clock frequency	f_{SCL}		0	-	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$		0.6	-	-	us
LOW period of the SCL clock	t_{LOW}	For all conditions	1.1	-	-	us
		vt_pix_clk_freq ≥ 6MHz	1.0	-	-	
HIGH period of the SCL clock	t_{HIGH}		0.6	-	-	us
Setup time for a repeated START condition	$t_{SU:STA}$		0.6	-	-	us
Data hold time	$t_{HD:DAT}$		0 (3)	-	0.9 (4)	us
Data setup time	$t_{SU:DAT}$		100 (2)	-	-	ns
Rise time of both SDA and SCL signals	t_r	C_B : from 10pF to 400pF	20 + 0.1 C_B (1)	-	300	ns
Fall time of both SDA and SCL signals	t_f	C_B : from 10pF to 400pF	20 + 0.1 C_B (1)	-	300	ns
Setup time for STOP condition	$t_{SU:STO}$		0.6	-	-	us
Bus free time between a STOP and START condition	t_{BUF}		1.3	-	-	us

[NOTE]
(1) C_B = Total capacitance of one bus line in pF
(2) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT}$ ≥250ns must be then met. This will be automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the low period of SCL signal, it must output the next data bit to the SDA line t_{rMAX} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2 bus specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{HD;DAT}$ has only to be met if the device does not the LOW period (t_{LOW})of the SCL signal.

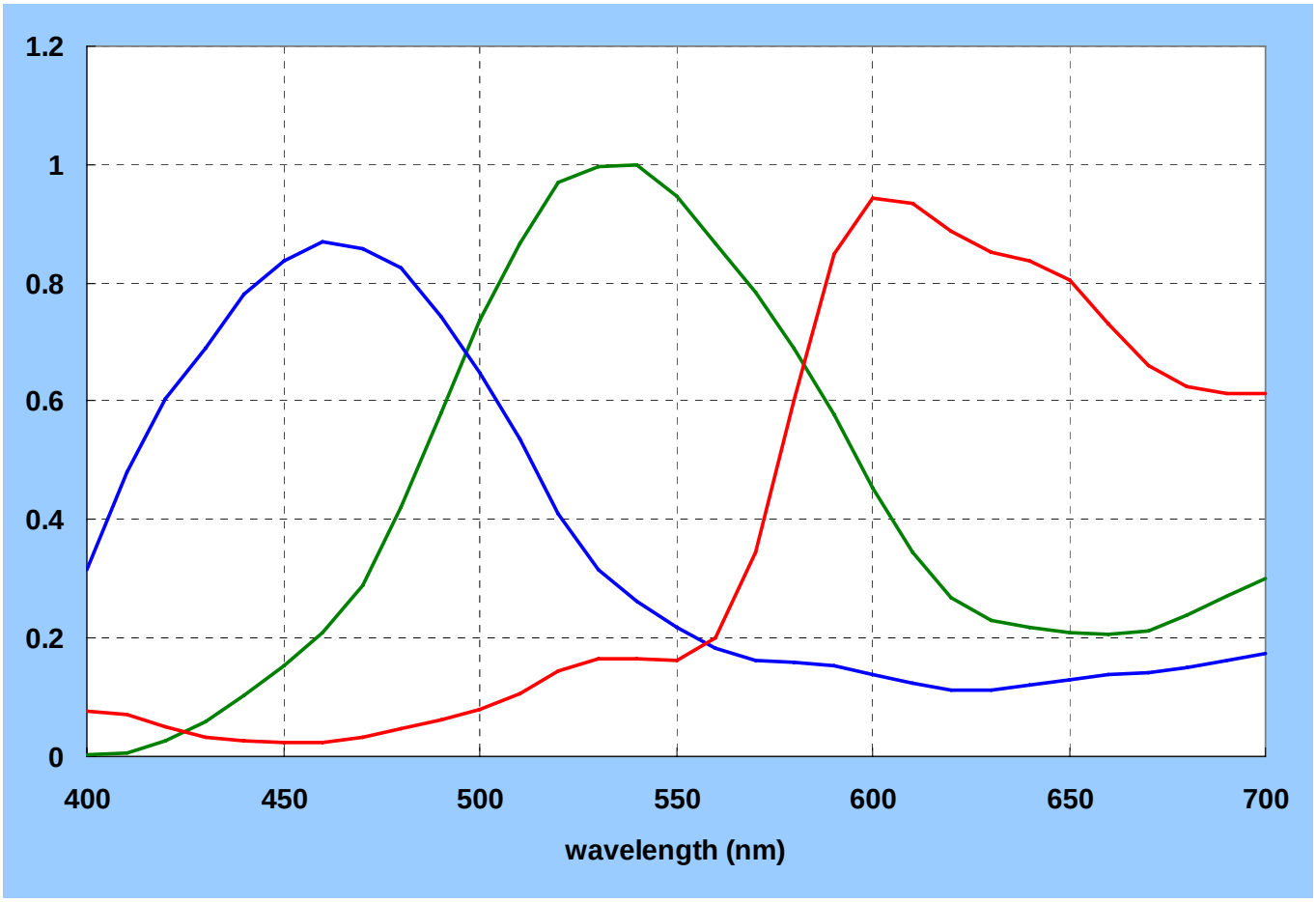
Table 12 : Imaging Characteristics

(All the values are obtained by using the SMIA 1.0 characterization method. Electrical operating conditions follow the recommended typical values : VANA=2.8V, VDIG=1.8V, T_A = 5/23/40°C, analog_gain = 1x for most of items except for PSRR.)

Characteristics	Min	Typ (5°C)	Typ (23°C)	Typ (40°C)	Max	Unit
Light Test						
Sensitivity	**0.11**	0.1448	0.1466	0.1482	-	1/Cdm $^{-2}$.sec
Photo Response Non-Uniformity	-	1.15	1.14	1.13	**1.3**	%
Module Response Non-Linearity (INL) (1)	-	0.0031	0.0033	0.0040	**0.006**	Code/FSD
Module Response Non- Linearity (DNL) (1)	-	0.0720	0.0760	0.0790	**0.21**	Code/FSD
SNR at 10 Cdm $^{-2}$	**32**	34.60	34.73	34.78	-	dB
SNR at 50 Cdm $^{-2}$	**34**	37.34	37.48	37.55	-	dB
SNR at 100 Cdm $^{-2}$	**35**	37.40	37.54	37.61	-	dB
SNR at 450 Cdm $^{-2}$	**35**	37.43	37.58	37.65	-	dB
Maximum illumination	**500000**	1016533	1004039	993295	-	Cdm $^{-2}$
Minimum illumination	-	0.214276	0.202105	0.199913	**0.34**	Cdm $^{-2}$
Image Lag	-	0.001	0.001	0.001	**0.004**	-
Dark Test						
Dynamic Range	**50**	53.65	54.10	54.21	-	dB
VFPN Level	-	0.000372	0.000368	0.000366	**0.00053**	Code/FSD
VFPN Max	-	0.001267	0.001280	0.001270	**0.0023**	Code/FSD
HFPN Level	-	0.001576	0.001574	0.001597	**0.0021**	Code/FSD
HFPN Max	-	0.001289	0.001272	0.001279	**0.00213**	Code/FSD
Temporal Noise	-	-55.49	-56.06	-56.23	**-54**	dB
Column Noise Level	-	-85.41	-86.61	-86.71	**-82**	dB
Column Noise Max	-	-78.65	-80.15	-80.4	**-72**	dB
Row Noise Level	-	-69.46	-69.93	-69.84	**-63**	dB
Row Noise Max	-	-65.1	-65.59	-65.58	**-58**	dB
Frame-to-Frame Flicker	-	0.00017	0.00015	0.00016	**0.003**	Codes
Dark Signal	-	-0.0043	-0.0036	-0.0017	**0.006**	Code/FSD.sec
Dark Signal Non-Uniformity	-	0.0088	0.0078	0.0083	**0.02**	Code/FSD.sec
PSRR @ 10kHz (2)	**35**	-	39.5	-	-	dB
PSRR @ 1MHz (2)	**25**	-	28.5	-	-	dB
PSRR @ 10MHz (2)	**50**	-	57.1	-	-	dB

[NOTE]
(1) Tested at Module-level (Except (1) and (2), other items are tested at Wafer-level.)
(2) Tested at analog_gain = 8x (max.) (Except (2), other items are tested at analog_gain = 1x.)
(3) Above specifications are covered for the full electrical operating range. (V_{ANA} = 2.4V ~ 2.9V, V_{DIG} = 1.7V ~ 1.9V)

Figure 21 : Spectral Response Specification



REGISTER DESCRIPTION

Configuration Registers 1

Index	Reset Value	Bits	Mnemonic	RW	Description
0x0000 0x0001	0x3B2F	[15:0]	model_id	RO	16-bit Sensor model number e.g. 552
0x0002	**0x84**	[7:0]	revision_number	RO	Silicon Revision Number **(dec:132)**
0x0003	0x09	[7:0]	manufacturer_id	RO	Manufacturer ID **(dec:9)**
0x0004	0x0A	[7:0]	smia_version	RO	9 - SMIA V0.9 10 - SMIA V1.0 11 - SMIA V1.1
0x0005	0xFF	[7:0]	frame_count	RO	8-bit (0-255) Frame counter value **(dec:255)**
0x0006	0x00	[7:0]	pixel_order	RO	Colour Pixel Order = {6'h00, image_orientation[1:0]} **(This register should apply the change of *image_orientation* .)**
0x0007			Reserved		
0x0008 0x0009	0x0040	[7:0]	data_pedestal	RO	Data pedestal – typically code 64 for 10-bit systems **(dec:64)** Refer to the Data Format Chapter = raw10mode ? 8'h40 : 8'h10 ;
0x000A					
0x000B					
0x000C	0x0A	[7:0]	pixel_depth	RO	8-bit, 10-bit or 12-bit pixel data = raw10mode? 8'h0A : 8'h08 ; **(dec:10)**
0x0040	0x01	[7:0]	frame_format_model_type	RO	
0x0041	0x12	[7:0]	frame_format_model_subtype	RO	
0x0042 0x0043	0x5650 x_output_size	[15:0]	frame_format_descriptor_0	RO	**(dec: 1616 columns)**
0x0044 0x0045	0x1002	[15:0]	frame_format_descriptor_1	RO	**(dec: 2 embedded lines)**
0x0046 0x0047	0x54C0 y_output_size	[15:0]	frame_format_descriptor_2	RO	**(dec: 1216 rows)**
0x0048 0x0049		[15:0]	frame_format_descriptor_3	RO	
0x004A 0x004B		[15:0]	frame_format_descriptor_4	RO	
0x004C 0x004D		[15:0]	frame_format_descriptor_5	RO	
0x004E 0x004F		[15:0]	frame_format_descriptor_6	RO	
0x0050 0x0051		[15:0]	frame_format_descriptor_7	RO	
0x0052 0x0053		[15:0]	frame_format_descriptor_8	RO	
0x0054 0x0055		[15:0]	frame_format_descriptor_9	RO	

Index	Reset Value	Bits	Mnemonic	RW	Description
0x0080 0x0081	0x0000	[15:0]	analogue_gain_capabiltiy	RO	Analogue Gain Capability 0 - single global alanlogue gain only 1 - separate channel alanlogue gains only
0x0082 0x0083			Reserved	RO	
0x0084 0x0085	0x0000	[15:0]	analogue_gain_code_min	RO	Minimum recommended analogue gain code **(dec:0)** Format : 16-bit unsigned integer
0x0086 0x0087	0x0070	[15:0]	analogue_gain_code_max	RO	Maximum recommended analogue gain code **(dec:8x)** Format : 16-bit unsigned integer
0x0088 0x0089	0x0001	[15:0]	analogue_gain_code_step	RO	Analogue gain code step size **(dec:1)** Format : 16-bit unsigned integer
0x008A 0x008B	0x0000	[15:0]	analogue_gain_type	RO	Analogue gain type **(dec:0)** Format : 16-bit unsigned integer
0x008C 0x008D	0x0000	[15:0]	analogue_gain_m0	RO	Analogue gain m0 constant **(dec:m0=0)** Format : 16-bit signed integer
0x008E 0x008F	0x0080	[15:0]	analogue_gain_c0	RO	Analogue gain c0 constant **(dec:c0=128)** Format ; 16-bit signed integer
0x0090 0x0091	0xFFFF	[15:0]	analogue_gain_m1	RO	Analogue gain m1 constant **(dec:m1=-1)** Format : 16-bit signed integer
0x0092 0x0093	0x0080	[15:0]	analogue_gain_c1	RO	Analogue gain c1 constant **(dec:c1=128)** Format : 16-bit signed integer
0x00C0	0x01	[7:0]	data_format_model_type	RO	0x01: 2-Byte Data Format
0x00C1	0x03	[7:0]	data_format_model_subtype	RO	Contains the number of data format descriptors used
0x00C2 0x00C3	0x0A0A	[15:0]	data_format_descriptor_0	RO	**ex) 0x0A0A: top 10-bit transmitted as RAW10**
0x00C4 0x00C5	0x0A08	[15:0]	data_format_descriptor_1	RO	ex) 0x0A08: top 10-bit compressed to 8-bit, and transmitted as RAW8
0x00C6 0x00C7	0x0808	[15:0]	data_format_descriptor_2	RO	**ex) 0x0808: top 8-bit transmitted as RAW8**
0x00C8 0x00C9	0x0000	[15:0]	data_format_descriptor_3	RO	
0x00CA 0x00CB	0x0000	[15:0]	data_format_descriptor_4	RO	
0x00CC 0x00CD	0x0000	[15:0]	data_format_descriptor_5	RO	
0x00CE 0x00CF	0x0000	[15:0]	data_format_descriptor_6	RO	

Configuration Registers 2

Index	Reset Value	Bits	Register Name	RW	Description
0x0100	0x00	[7:0]	mode_select	RW	Mode Select 0 – Software Standby 1 - Streaming Refer to Operating Modes Chapter
0x0101	0x00	[7:0]	image_orientation	RW	Image orientation i.e. horizontal mirror and vertical flip Refer to Video Timing Chapter
0x0102			Reserved		
0x0103	0x00	[7:0]	software_reset	RW	Software reset Refer to Operating Modes Chapter
0x0104	0x00	[7:0]	grouped_parameter_hold	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0 – consume as normal 1 - hold Refer to Integration Time and Gain Control Chapter
0x0105	0x00	[7:0]	mask_corrupted_frames	RW	Refer to Integration Time and Gain Control Chapter
0x0110	0x00	[7:0]	CCP2_channel_identifier	RW	Channel Identifier Value for CCP2 embedded codes Valid Range: 0-7
0x0111	0x00	[7:0]	CCP2_signalling_mode	RW	0 – Data/Clock Signalling 1 - Data/Strobe Signalling
0x0112 0x0113	0x0A0A	[15:0]	CCP_data_format	RW	CCP Data Format 0x0808: Top 8-b of pixel data,RAW8 0x0A08: 10-b to 8-b compression, RAW8 0x0A0A: Top 10-b of pixel data, RAW10
0x0120	0x00	[7:0]	gain_mode	RW	0 – Global Analogue Gain (Default) 1 – Per Channel Analogue Gain (Only if sensor supports it) Refer to Integration Time and Gain Chapter
0x0200 0x0201	0x06CA	[15:0]	fine_integration_time	RW	Fine integration time (pixels) **(dec:1738)** Format: 16-bit unsigned integer
0x0202 0x0203	0x04DF	[15:0]	coarse_integration_time	RW	Coarse integration time (lines) **(dec:1247)** Format: 16-bit unsigned integer
0x0204 0x0205	0x0000	[15:0]	analogue_gain_code_global	RW	Global Analogue Gain Code **(dec:1x)** Format: 16-bit unsigned integer
0x0206 0x0207	0x0000	[15:0]	analogue_gain_code_greenR	RW	Analogue Gain Code **(dec:1x)** Format: 16-bit unsigned integer

Index	Reset Value	Bits	Register Name	RW	Description
0x0208 0x0209	0x0000	[15:0]	analogue_gain_code_red	RW	Red Channel Analogue Gain Code **(dec:1x)** Format: 16-bit unsigned integer
0x020A 0x020B	0x0000	[15:0]	analogue_gain_code_blue	RW	Blue Channel Analogue Gain Code **(dec:1x)** Format: 16-bit unsigned integer
0x020C 0x020D	0x0000	[15:0]	analogue_gain_code_greenB	RW	Green (Blue Row) Analogue Gain Code **(dec:1x)** Format: 16-bit unsigned integer
0x020E 0x020F	0x0100	[15:0]	digital_gain_greenR	RW	Green (Red Row) channel digital gain value **(dec:1x)** Format: 16-bit unsigned iReal
0x0210 0x0211	0x0100	[15:0]	digital_gain_red	RW	Red channel digital gain value **(dec:1x)** Format: 16-bit unsigned iReal
0x0212 0x0213	0x0100	[15:0]	digital_gain_blue	RW	Blue channel digital gain value **(dec:1x)** Format: 16-bit unsigned iReal
0x0214 0x0215	0x0100	[15:0]	digital_gain_greenB	RW	Green (Blue Row) channel digital gain value **(dec:1x)** Format: 16-bit unsigned iReal
0x0300 0x0301	0x000A	[15:0]	vt_pix_clk_div	RW	Video Timing Pixel Clock Divider **(dec:10)** Format: 16-bit unsigned integer
0x0302 0x0303	0x0004	[15:0]	vt_sys_clk_div	RW	Video Timing System Clock Divider Value **(dec:4)** Format: 16-bit unsigned integer
0x0304 0x0305	0x0004	[15:0]	pre_pll_clk_div	RW	Pre PLL clock Divider Value **(dec:4)** Format: 16-bit unsigned integer
0x0306 0x0307	0x00C8	[15:0]	pll_multiplier	RW	PLL multiplier Value **(dec:200)** Format: 16-bit unsigned integer
0x0308 0x0309	0x000A	[15:0]	op_pix_clk_div	RO	Output Pixel Clock Divider **(dec:10)** Format: 16-bit unsigned integer
0x030A 0x030B	0x0004	[15:0]	op_sys_clk_div	RW	Output System Clock Divider Value **(dec:4)** Format: 16-bit unsigned integer
0x0340 0x0341	0x04DF	[15:0]	frame_length_lines	RW	Frame Length **(dec:1247)** Format: 16-bit unsigned integer (Lines)
0x0342 0x0343	0x06CA	[15:0]	line_length_pck	RW	Line Length **(dec:1738)** Format: 16-bit unsigned integer (Pixel Clocks)
0x0344 0x0345	0x0006	[15:0]	x_addr_start	RW	X-address of the top left corner of the visible pixel data **(dec:6)** Format: 16-bit unsigned integer (Pixels)
0x0346 0x0347	0x0004	[15:0]	y_addr_start	RW	Y-address of the top left corner of the visible pixel data **(dec:4)** Format: 16-bit unsigned integer (Lines)
0x0348 0x0349	0x064D	[15:0]	x_addr_end	RW	X-address of the bottom right corner of the visible pixel data **(dec:1613)** Format: 16-bit unsigned integer (Pixels)

Index	Reset Value	Bits	Register Name	RW	Description
0x034A 0x034B	0x04B7	[15:0]	y_addr_end	RW	Y-address of the bottom right corner of the visible pixel data **(dec:1207)** Format: 16-bit unsigned integer (Lines)
0x034C 0x034D	0x0650	[15:0]	x_output_size	RW	Width of image data output from the sensor module **(dec:1616)** Format: 16-bit unsigned integer (Pixels)
0x034E 0x034F	0x04C0	[15:0]	y_output_size	RW	Height of image data output from the sensor module **(dec:1216)** Format: 16-bit unsigned integer (Lines)
0x0380 0x0381	0x0001	[15:0]	x_even_inc	RW	Increment for even pixels – 0, 2, 4 etc **(dec:1)** Format: 16-bit unsigned integer
0x0382 0x0383	0x0001	[15:0]	x_odd_inc	RW	Increment for odd pixels – 1, 3, 5 etc **(dec:1)** Format: 16-bit unsigned integer
0x0384 0x0385	0x0001	[15:0]	y_even_inc	RW	Increment for even pixels – 0, 2, 4 etc **(dec:1)** Format: 16-bit unsigned integer
0x0386 0x0387	0x0001	[15:0]	y_odd_inc	RW	Increment for odd pixels – 1, 3, 5 etc **(dec:1)** Format: 16-bit unsigned integer

Configuration Registers 3

Index	Reset Value	Bits	Register Name	RW	Description
0x0400 0x0401	0x0000	[15:0]	Scaling_mode	RW	0 – No scaling 1 – Horizontal Scaling 2 – Full Scaling (both horizontal and vertical)
0x0402 0x0403	0x0001	[15:0]	Spatial_sampling	RW	0 – Bayer Sampling 1 – Co-sited 2 – Reserved
0x0404 0x0405	0x0010	[15:0]	scale_m	RW	Down scale factor: M component Range: 1 to 16 upwards **(dec:16)** Format: 16-bit unsigned integer
0x0406 0x0407	0x0010	[15:0]	scale_n	RW	Down scale factor: N component Value: 16 (fixed) **(dec:16)** Format: 16-bit unsigned integer
0x0500 0x0501	0x0000	[15:0]	compression_mode	RW	1 – DPCM/PCM Compression - Simple Predictor 2 – DPCM/PCM – Advanced Predictor **(dec:0 – no compression)**
0x0600 0x0601	0x0000	[15:0]	test_pattern_mode	RW	
0x0602 0x0603	0x0200	[15:0]	test_data_red	RW	**(dec:512)**
0x0604 0x0605	0x0200	[15:0]	test_data_greenR	RW	**(dec:512)**
0x0606 0x0607	0x0200	[15:0]	test_data_blue	RW	**(dec:512)**
0x0608 0x0609	0x0200	[15:0]	test_data_greenB	RW	**(dec:512)**
0x060A 0x060B	0x0000	[15:0]	horizontal_cursor_width	RW	**(dec:0 – no h-cursor)**
0x060C 0x060D	0x0100	[15:0]	horizontal_cursor_position	RW	**(dec:256)**
0x060E 0x060F	0x0000	[15:0]	vertical_cursor_width	RW	**(dec:0 – no v-cursor)**
0x0610 0x0611	0x0100	[15:0]	vertical_cursor_position	RW	**(dec:256)**
0x0700 0x0701	0x0510	[15:0]	fifo_water_mark_pixels	RW	**(dec:1296)**

Parameter Limit Registers – [0x1000-0x1FFF] (Read Only and Static)

Index	Reset Value	Bits	Register Name	RW	Description
0x1000 0x1001	0x0001	[15:0]	integration_time_capability	RO	0 – coarse integration but NO fine integration 1 – course and smooth (1 pixel) fine integration
0x1002 0x1003	0x0000	[15:0]	Reserved	RO	
0x1004 0x1005	0x0000	[15:0]	coarse_integration_time_min	RO	Lines **(dec:0)** Format: 16-bits unsigned integer
0x1006 0x1007	0x0002	[15:0]	coarse_integration_time_max_margin	RO	(Current frame length – current max coarse exp) **(dec:2)** Format: 16-bits unsigned integer
0x1008 0x1009	0x00DD	[15:0]	fine_integration_time_min	RO	Pixels **(dec:221)** Format: 16-bits unsigned integer
0x100A 0x100B	0x0002	[15:0]	fine_integration_time_max_margin	RO	(Current line length – current max fine exp) **(dec:2)** Format: 16-bits unsigned integer
0x1080 0x1081	0x0001	[15:0]	digital_gain_capability	RO	0 – none 1 – per channel digital gain
0x1082 0x1083	0x0000	[15:0]	Reserved	RO	
0x1084 0x1085	0x0100	[15:0]	digital_gain_min	RO	Minimum recommended digital gain value **(dec:1x)** Format: 16-bit unsigned 8.8 fixed point number
0x1086 0x1087	0x0800	[15:0]	digital_gain_max	RO	Maximum recommended digital gain value **(dec:8x)** Format: 16-bit unsigned 8.8 fixed point number
0x1088 0x1089	0x0001	[15:0]	digital_gain_step_size	RO	Digital gain step size **(dec:1/256)** Format: 16-bit unsigned 8.8 fixed point number
0x1100 0x1101 0x1102 0x1103	0x40C0_0000	[31:0]	min_ext_clk_freq_mhz	RO	Minimum external clock frequency Format: IEEE 32-bit float Units: MHz **(dec:6MHz)**
0x1104 0x1105 0x1106 0x1107	0x41D8_0000	[31:0]	max_ext_clk_freq_mhz	RO	Maximum external clock frequency **(dec:27MHz)** Format: IEEE 32-bit float Units: MHz
0x1108 0x1109	0x0001	[15:0]	min_pre_pll_clk_div	RO	Minimum Pre PLL divider value **(dec:1)** Format: 16-bit unsigned integer
0x110A 0x110B	0x001A	[15:0]	max_pre_pll_clk_div	RO	Maximum Pre PLL divider value **(dec:26)** Format: 16-bit unsigned integer

Index	Reset Value	Bits	Register Name	RW	Description
0x110C 0x110D 0x110E 0x110F	0x3F80_0000	[31:0]	min_pll_ip_freq_mhz	RO	Minimum PLL input clock frequency **(dec:1MHz)** Format: IEEE 32-bit float Units: MHz
0x1110 0x1111 0x1112 0x1113	0x40C0_0000	[31:0]	max_pll_ip_freq_mhz	RO	Maximum PLL input clock frequency **(dec:6MHz)** Format: IEEE 32-bit float Units: MHz
0x1114 0x1115	0x0036	[15:0]	min_pll_multiplier	RO	Minimum PLL multiplier **(dec:54)** Format: 16-bit unsigned integer
0x1116 0x1117	0x028A	[15:0]	max_pll_multiplier	RO	Maximum PLL multiplier **(dec:650)** Format: 16-bit unsigned integer
0x1118 0x1119 0x111A 0x111B	0x43A2_0000	[31:0]	min_pll_op_freq_mhz	RO	Minimum PLL output clock frequency **(dec:324MHz)** Format: IEEE 32-bit float Units: MHz
0x111C 0x111D 0x111E 0x111F	0x4422_8000	[31:0]	max_pll_op_freq_mhz	RO	Maximum PLL output clock frequency **(dec:650MHz)** Format: IEEE 32-bit float Units: MHz
0x1120 0x1121	0x0001	[15:0]	min_vt_sys_clk_div	RO	Minimum video timing system clock divider value **(dec:1)** Format: 16-bit unsigned integer
0x1122 0x1123	0x0008	[15:0]	max_vt_sys_clk_div	RO	Maximum video timing system clock divider value **(dec:8)** Format: 16-bit unsigned integer
0x1124 0x1125 0x1126 0x1127	0x4222_0000	[31:0]	min_vt_sys_clk_freq_mhz	RO	Minimum video timing system clock frequency **(dec:40.5MHz)** Format: IEEE 32-bit float Units: MHz
0x1128 0x1129 0x112A 0x112B	0x4422_8000	[31:0]	max_vt_sys_clk_freq_mhz	RO	Maximum video timing system clock frequency **(dec:650MHz)** Format: IEEE 32-bit float Units: MHz
0x112C 0x112D 0x112E 0x112F	0x4081_999A	[31:0]	min_vt_pix_clk_freq_mhz	RO	Minimum video timing pixel clock frequency **(dec:4.05MHz)** Format: IEEE 32-bit float Units: MHz
0x1130 0x1131 0x1132 0x1133	0x4282_0000	[31:0]	max_vt_pix_clk_freq_mhz	RO	Maximum video timing pixel clock frequency **(dec:65MHz)** Format: IEEE 32-bit float Units: MHz

Index	Reset Value	Bits	Register Name	RW	Description
0x1134 0x1135	0x0004	[15:0]	min_vt_pix_clk_div	RO	Minimum video timing pixel clock divider value **(dec:4)** Format: 16-bit unsigned integer
0x1136 0x1137	0x000A	[15:0]	max_vt_pix_clk_div	RO	Maximum video timing pixel clock divider value **(dec:10)** Format: 16-bit unsigned integer
0x1140 0x1141	0x00D0	[15:0]	min_frame_length_lines	RO	Minimum Frame Length allowed. Value both sensor dependent Units: Lines **(dec:208)** Format: 16-bit unsigned integer
0x1142 0x1143	0xFFFF	[15:0]	max_frame_length_lines	RO	Maximum possible number of lines per Frame. **(dec:65535)** Value sensor dependent Format: 16-bit unsigned integer Units: Lines
0x1144 0x1145	0x06CA	[15:0]	min_line_length_pck	RO	Minimum Line Length allowed. Value sensor dependent **(dec:1738)** Format: 16-bit unsigned integer Units: Pixel Clocks
0x1146 0x1147	0xFFFF	[15:0]	max_line_length_pck	RO	Maximum possible number of pixel clocks per line. **(dec:65535)** Value sensor dependent Format: 16-bit unsigned integer Units: Pixel Clocks
0x1148 0x1149	0x0062	[15:0]	min_line_blanking_pck	RO	Minimum line blanking time in pixel clocks **(dec:98)** Format: 16-bit unsigned integer Units: Pixel Clocks
0x114A 0x114B	0x000C	[15:0]	min_frame_blanking_lines	RO	Minimum frame blanking in video tming lines **(dec:12)** Format: 16-bit unsigned integer Units: Pixel Clocks
0x1160 0x1161	0x0001	[15:0]	min_op_sys_clk_div	RO	Minimum output system clock divider value **(dec:1)** Format: 16-bit unsigned integer
0x1162 0x1163	0x0008	[15:0]	max_op_sys_clk_div	RO	Maximum output system clock divider value **(dec:8)** Format: 16-bit unsigned integer
0x1164 0x1165 0x1166 0x1167	0x4222_0000	[31:0]	min_op_sys_ck_clk_freq_mhz	RO	Minimum output system clock frequency **(dec:40.5MHz)** Format: IEEE 32-bit float Units: MHz
0x1168 0x1169 0x116A 0x116B	0x4422_8000	[31:0]	max_op_sys_clk_freq_mhz	RO	Maximum output system clock frequency **(dec:650MHz)** Format: IEEE 32-bit float Units: MHz

Index	Reset Value	Bits	Register Name	RW	Description
0x116C 0x116D	0x0008	[15:0]	min_op_pix_clk_div	RO	Minimum output pixel clock divider value **(dec:8)** Format: 16-bit unsigned integer
0x116E 0x116F	0x000A	[15:0]	max_op_pix_clk_div	RO	Maximum output pixel clock divider value **(dec:10)** Format: 16-bit unsigned integer
0x1170 0x1171 0x1172 0x1173	0x4081_999A	[31:0]	min_op_pix_clk_freq_mhz	RO	Minimum output pixel clock frequency **(dec:4.05MHz)** Format: IEEE 32-bit float Units: MHz
0x1174 0x1175 0x1176 0x1177	0x4282_0000	[31:0]	max_op_pix_clk_freq_mhz	RO	Maximum output pixel clock frequency **(dec:65MHz)** Format: IEEE 32-bit float Units: MHz
0x1180 0x1181	0x0000	[15:0]	x_addr_min	RO	**(dec:0)**
0x1182 0x1183	0x0000	[15:0]	y_addr_min	RO	**(dec:0)**
0x1184 0x1185	0x0653	[15:0]	x_addr_max	RO	**(dec:1619)**
0x1186 0x1187	0x04BF	[15:0]	y_addr_max	RO	**(dec:1215)**
0x1188 0x1189	0x0100	[15:0]	min_x_output_size	RO	**(dec:256)**
0x118A 0x118B	0x00C0	[15:0]	min_y_output_size	RO	**(dec:195)**
0x118C 0x118D	0x0660	[15:0]	max_x_output_size	RO	**(dec:1632)**
0x118E 0x118F	0x04D0	[15:0]	max_y_output_size	RO	**(dec:1232)**
0x11C0 0x11C1	0x0001	[15:0]	min_even_inc	RO	Minimum Increment for even pixels **(dec:1)** Format: 16-bit unsigned integer (static)
0x11C2 0x11C3	0x000B	[15:0]	max_even_inc	RO	Maximum increment for even pixels **(dec:11)** Format: 16-bit unsigned integer (static)
0x11C4 0x11C5	0x0001	[15:0]	min_odd_inc	RO	Minimum Increment for odd pixels **(dec:1)** Format: 16-bit unsigned integer (static)
0x11C6 0x11C7	0x000B	[15:0]	max_odd_inc	RO	Maximum Increment for odd pixels **(dec:11)** Format: 16-bit unsigned integer (static)
0x1200 0x1201	0x0002	[15:0]	scaling_capability	RO	0 – None 1 – Horizontal 2 – Full (Horizontal & Vertical) Format: 16-bit unsigned integer

Index	Reset Value	Bits	Register Name	RW	Description
0x1202 0x1203	0x0000	[15:0]	reserved	RO	
0x1204 0x1205	0x0010	[15:0]	scaler_m_min	RO	Down scale factor: Minimum M value Value is always 16 **(dec:16)** Format: 16-bit unsigned integer
0x1206 0x1207	0x0060	[15:0]	scaler_m_max	RO	Down scale factor: Maximum M value **(dec:96)** Format: 16-bit unsigned integer
0x1208 0x1209	0x0010	[15:0]	scaler_n_min	RO	Down scale factor: Minimum N value Value is always 16 **(dec:16)** Format: 16-bit unsigned integer
0x120A 0x120B	0x0010	[15:0]	scaler_n_max	RO	Down scale factor: Maximum N value Value is always 16 **(dec:16)** Format: 16-bit unsigned integer
0x1300 0x1301	0x0001	[15:0]	compression_capability	RW	0 – No Compression 1 – DPCM/PCM Compression
0x1400 0x1401	**0x023F**	[15:0]	**matrix_element_RedInRed**	RO	Colour matrix parameter for Red in Red **(dec:2.246)** Format: 16-bit signed iReal
0x1402 0x1403	**0xFF0B**	[15:0]	**matrix_element_GreenInRed**	RO	Colour matrix parameter for Green in Red **(dec:-0.957)** Format: 16-bit signed iReal
0x1404 0x1405	**0xFFB6**	[15:0]	**matrix_element_BlueInRed**	RO	Colour matrix parameter for Blue in Red **(dec:-0.289)** Format: 16-bit signed iReal
0x1406 0x1407	**0xFF60**	[15:0]	**matrix_element_RedInGreen**	RO	Colour matrix parameter for Red in Green **(dec:-0.625)** Format: 16-bit signed iReal
0x1408 0x1409	**0x0236**	[15:0]	**matrix_element_GreenInGreen**	RO	Colour matrix parameter for Green in Green **(dec:2.211)** Format: 16-bit signed iReal
0x140A 0x140B	**0xFF6A**	[15:0]	**matrix_element_BlueInGreen**	RO	Colour matrix parameter for Blue in Green **(dec:-0.586)** Format: 16-bit signed iReal
0x140C 0x140D	**0x0002**	[15:0]	**matrix_element_RedInBlue**	RO	Colour matrix parameter for Red in Blue **(dec:0.008)** Format: 16-bit signed iReal
0x140E 0x140F	**0xFFA9**	[15:0]	**matrix_element_GreenInBlue**	RO	Colour matrix parameter for Green in Blue **(dec:-1.340)** Format: 16-bit signed iReal
0x1410 0x1411	**0x0255**	[15:0]	**matrix_element_BlueInBlue**	RO	Colour matrix parameter for Blue in Blue **(dec:2.332)** Format: 16-bit signed iReal
0x1500 0x1501	0x0660	[15:0]	fifo_size_pixels	RO	FIFO size in pixels (0 = no FIFO present) **(dec:1632)** Format : 16-bit unsigned integer

Manufacturer Specific Registers – [0x3000-0x3FFF] (Read/Write)

Index	Reset Value	Bits	Register Name	RW	Description
0x3000	0x35	[6:0]	Reserved	RW	
0x3001	0x02	[4:0]	Reserved	RW	
0x3002	0x29	[7:0]	Reserved	RW	
0x3003	0x01	[1:0]	Reserved	RW	
0x3004	0x064E	[15:0]	Reserved	RW	
0x3005					
0x3006	0x0012	[15:0]	Reserved	RW	
0x3007					
0x3008	0x85F6	[11:0]	Reserved	RW	
0x3009					
0x3010	0x52	[6:0]	Reserved	RW	
0x3011	0x00	[3:0]	Reserved	RW	
0x3012	0xDF	[7:0]	Reserved	RW	
0x3013	0xC0	[7:0]	Reserved	RW	
0x3014	0xD9	[7:0]	Reserved	RW	
0x3015	0x00	[0]	Reserved	RW	
0x3016	**0x85**	[7:0]	**dark_level_offset**	RW	
0x3017	0x80	[7:0]	Reserved	RW	
0x3018	0x80	[7:0]	Reserved	RW	
0x3019	0x80	[7:0]	Reserved	RW	
0x301A	0x80	[7:0]	Reserved	RW	
0x301B	0x80	[7:0]	Reserved	RW	
0x3020	0x00	[0]	Reserved	RW	
0x3021	**0x12**	[4:0]	**adc_range_control**	RW	
0x3022	0x1F	[4:0]	Reserved	RW	
0x3023	0x1F	[4:0]	Reserved	RW	
0x3024	0x1F	[4:0]	Reserved	RW	
0x3025	0x1F	[4:0]	Reserved	RW	
0x3030	0x00	[6:0]	Reserved	RW	
0x3032	0x0000	[11:0]	Reserved	RW	
0x3033					
0x3034	0x0000	[11:0]	Reserved	RW	
0x3035					
0x3036	0x0000	[11:0]	Reserved	RW	
0x3037					
0x3038	0x0000	[11:0]	Reserved	RW	
0x3039					
0x303A	0x0000	[11:0]	Reserved	RW	
0x303B					
0x303C	0x0000	[11:0]	Reserved	RW	
0x303D					
0x303E	0x0000	[11:0]	Reserved	RW	

Index	Reset Value	Bits	Register Name	RW	Description
0x303F					
0x3040 0x3041	0x0000	[11:0]	Reserved	RW	
0x3042 0x3043	0x0000	[11:0]	Reserved	RW	
0x3044 0x3045	0x0000	[11:0]	Reserved	RW	
0x3046 0x3047	0x0000	[11:0]	Reserved	RW	
0x3048 0x3049	0x0000	[11:0]	Reserved	RW	
0x304A 0x304B	0x0000	[11:0]	Reserved	RW	
0x304C 0x304D	0x0000	[11:0]	Reserved	RW	
0x304E 0x304F	0x0000	[11:0]	Reserved	RW	
0x3050 0x3051	0x0000	[11:0]	Reserved	RW	
0x3080	0x10	[7:0]	Reserved	RW	
0x3081	**0x10**	[4:0]	**adlc**	RW	
0x3082	0x00	[7:0]	Reserved	RW	
0x3083	0x00	[7:0]	Reserved	RW	
0x3084	0x09	[3:0]	Reserved	RW	
0x3085	0x00	[3:0]	Reserved	RW	
0x3086	0x33	[7:0]	Reserved	RW	
0x3087	0x45	[7:0]	Reserved	RW	
0x3088	0x00	[6:0]	Reserved	RW	
0x3089	0x08	[4:0]	Reserved	RW	
0x308A			Reserved		
0x3090	0x08	[7:0]	Reserved	RW	
0x3091	0x04	[7:0]	Reserved	RW	
0x3092	0x05	[5:0]	Reserved	RW	
0x3093	0x88	[7:0]	Reserved	RW	
0x3094	0x05	[6:0]	Reserved	RW	
0x3095	0x80	[1:0]	Reserved	RW	
0x3096	0x00	[7:0]	Reserved	RW	
0x3097	0x08	[7:0]	Reserved	RW	
0x3098	0x08	[3:0]	Reserved	RW	
0x3099	0x00	[7:0]	Reserved	RW	
0x30A0	0x01	[7:0]	Reserved	RW	
0x30A1	0xA5	[7:0]	Reserved	RW	
0x30A2	0x00	[7:0]	Reserved	RW	
0x30A3	0x00	[7:0]	Reserved	RW	

EMBEDDED DATA CONTENTS

When embedded data is enabled in the output image, the first two rows of the output image contain register values that are appropriate for the output image. The format of this data is shown in below table. In the table, 8-bit and 10-bit versions of the data are shown; when a 10-bit format is used, the high 8-bits hold the data byte and the low two bits are set to 01. Register values that are shown as "??" indicates dynamic value and it may change from frame to frame or may change by the effect of other register settings.

Offset	Row 0			Row 1		
	8-bit	Reg. Addr	Comment	8-bit	Reg. Addr	Comment
0	0x0A	—	2-byte tagged data format (embedded data)	0x0A	—	2-byte tagged data format (embedded data)
1	0xAA	—	CCI register index MSB	0xAA	—	CCI register index MSB
2	0x00	—	Address 00xx	0x03	—	Address 03xx
3	0xA5	—	CCI register index LSB	0xA5	—	CCI register index LSB
4	0x00	—	Address xx00	0x00	—	Address xx00
5	0x5A	—	auto_increment	0x5A	—	auto_increment
6	0x3B	0x0000	model_id_hi	0x00	0x0300	vt_pix_clk_div_hi
7	0x5A	—		0x5A	—	
8	0x2F	0x0001	model_id_lo	??	0x0301	vt_pix_clk_div_lo
9	0x5A	—		0x5A	—	
10	0x84	0x0002	revision_number (EVT2.2)	0x00	0x0302	vt_sys_clk_div_hi
11	0x5A	—		0x5A	—	
12	0x09	0x0003	manufacturer_id	??	0x0303	vt_sys_clk_div_lo
13	0x5A	—		0x5A	—	
14	0x0A	0x0004	smia_version	0	0x0304	pre_pll_clk_div_hi
15	0x5A	—		0x5A	—	
16	??	0x0005	frame_count	??	0x0305	pre_pll_clk_div_lo
17	0x5A	—		0x5A	—	
18	??	0x0006	pixel_order	??	0x0306	pll_multiplier_hi
19	0x55	—	auto_increment-null data	0x5A	—	
20	0x07	0x0007	Null Data	??	0x0307	pll_multiplier_lo
21	0x5A	—	auto_increment	0x5A	—	
22	0x00	0x0008	data_pedestal_hi	0x00	0x0308	op_pix_clk_div_hi
23	0x5A	—		0x5A	—	
24	0x40	0x0009	data_pedestal_lo	??	0x0309	op_pix_clk_div_lo
25	0xA5	—	CCI register index LSB	0x5A	—	
26	0x0C	—	Address xx0C	0x00	0x030A	op_sys_clk_div_hi
27	0x5A	—	auto_increment	0x5A	—	
28	0x0A	0x000C	pixel_depth	??	0x030B	op_sys_clk_div_lo
29	0xA5	—	CCI register index LSB	0xA5	—	CCI register index LSB
30	0x40	—	Address xx40	0x40	—	Address xx40

Offset	Row 0			Row 1		
	8-bit	Reg. Addr	Comment	8-bit	Reg. Addr	Comment
31	0x5A	—	auto_increment	0x5A	—	auto_increment
32	0x01	0x0040	frame_format_model_type	??	0x0340	frame_length_lines_hi
33	0x5A	—		0x5A	—	
34	0x12	0x0041	frame_format_model_subtype	??	0x0341	frame_length_lines_lo
35	0x5A	—		0x5A	—	
36	0x56	0x0042	frame_format_descriptor_0_hi	??	0x0342	line_length_pck_hi
37	0x5A	—		0x5A	—	
38	0x50	0x0043	frame_format_descriptor_0_lo	??	0x0343	line_length_pck_lo
39	0x5A	—		0x5A	—	
40	0x10	0x0044	frame_format_descriptor_1_hi	??	0x0344	x_addr_start_hi
41	0x5A	—		0x5A	—	
42	0x02	0x0045	frame_format_descriptor_1_lo	??	0x0345	x_addr_start_lo
43	0x5A	—		0x5A	—	
44	0x54	0x0046	frame_format_descriptor_2_hi	??	0x0346	y_addr_start_hi
45	0x5A	—		0x5A	—	
46	0xC0	0x0047	frame_format_descriptor_2_lo	??	0x0347	y_addr_start_lo
47	0x5A	—		0x5A	—	
48	0x00	0x0048	frame_format_descriptor_3 hi	??	0x0348	x_addr_end_hi
49	0x5A	—		0x5A	—	
50	0x00	0x0049	frame_format_descriptor_3 lo	??	0x0349	x_addr_end_lo
51	0x5A	—		0x5A	—	
52	0x00	0x004A	frame_format_descriptor_4 hi	??	0x034A	y_addr_end_hi
53	0x5A	—		0x5A	—	
54	0x00	0x004B	frame_format_descriptor_4 lo	??	0x034B	y_addr_end_lo
55	0x5A	—		0x5A	—	
56	0x00	0x004C	frame_format_descriptor_5 hi	??	0x034C	x_output_size_hi
57	0x5A	—		0x5A	—	
58	0x00	0x004D	frame_format_descriptor_5 lo	??	0x034D	x_output_size_lo
59	0x5A	—		0x5A	—	
60	0x00	0x004E	frame_format_descriptor_6 hi	??	0x034E	y_output_size_hi
61	0x5A	—		0x5A	—	
62	0x00	0x004F	frame_format_descriptor_6 lo	??	0x034F	y_output_size_lo
63	0x5A	—		0xA5	—	CCI register index LSB
64	0x00	0x0050	frame_format_descriptor_7 hi	0x80	—	Address xx80
65	0x5A	—		0x5A	—	auto increment
66	0x00	0x0051	frame_format_descriptor_7 lo	0x00	0x0380	x_even_inc_hi
67	0x5A	—		0x5A	—	
68	0x00	0x0052	frame_format_descriptor_8 hi	??	0x0381	x_even_inc_lo

Offset	Row 0			Row 1		
	8-bit	Reg. Addr	Comment	8-bit	Reg. Addr	Comment
69	0x5A	—		0x5A	—	
70	0x00	0x0053	frame_format_descriptor_8 lo	0x00	0x0382	x_odd_inc_hi
71	0x5A	—		0x5A	—	
72	0x00	0x0054	frame_format_descriptor_9 hi	??	0x0383	x_odd_inc_lo
73	0x5A	—		0x5A	—	
74	0x00	0x0055	frame_format_descriptor_9 lo	0x00	0x0384	y_even_inc_hi
75	0x5A	—		0x5A	—	
76	0x00	0x0056	frame_format_descriptor_10 hi	??	0x0385	y_even_inc_lo
77	0x5A	—		0x5A	—	
78	0x00	0x0057	frame_format_descriptor_10 lo	0x00	0x0386	y_odd_inc_hi
79	0x5A	—		0x5A	—	
80	0x00	0x0058	frame_format_descriptor_11 hi	??	0x0387	y_odd_inc_lo
81	0x5A	—		0xAA	—	CCI register index MSB
82	0x00	0x0059	frame_format_descriptor_11 lo	0x04	—	Address 04xx
83	0x5A	—		0xA5	—	CCI register index LSB
84	0x00	0x005A	frame_format_descriptor_12 hi	0x00	—	Address xx00
85	0x5A	—		0x5A	—	auto_increment
86	0x00	0x005B	frame_format_descriptor_12 lo	0x00	0x0400	scaling_mode_hi
87	0xA5	—	CCI register index LSB	0x5A	—	
88	0x80	—	Address xx80	??	0x0401	scaling_mode_lo
89	0x5A	—	auto increment	0x5A	—	
90	0x00	0x0080	analogue_gain_capability_hi	0x00	0x0402	spatial_sampling_hi
91	0x5A	—		0x5A	—	
92	0x00	0x0081	analogue_gain_capability_lo	??	0x0403	spatial_sampling_lo
93	0xA5	—	CCI register index LSB	0x5A	—	
94	0x84	—	Address xx84	??	0x0404	scale_m_hi
95	0x5A	—	auto increment	0x5A	—	
96	0x00	0x0084	analogue_gain_code_min_hi	??	0x0405	scale_m_lo
97	0x5A	—		0x5A	—	
98	0x00	0x0085	analogue_gain_code_min_lo	0x00	0x0406	scale_n_hi
99	0x5A	—		0x5A	—	
100	0x00	0x0086	analogue_gain_code_max_hi	0x10	0x0407	scale_n_lo
101	0x5A	—		0xAA	—	CCI register index MSB
102	0x70	0x0087	analogue_gain_code_max_lo	0x05	—	Address 05xx
103	0x5A	—		0xA5	—	CCI register index LSB
104	0x00	0x0088	analogue_gain_code_step_hi	0x00	—	Address xx00
105	0x5A	—		0x5A	—	auto_increment
106	0x01	0x0089	analogue_gain_code_step_lo	0x00	0x0500	compression_mode_hi

Offset	Row 0			Row 1		
	8-bit	Reg. Addr	Comment	8-bit	Reg. Addr	Comment
107	0x5A	—		0x5A	—	
108	0x00	0x008A	analogue_gain_type_hi	??	0x0501	compression_mode_lo
109	0x5A	—		0xAA	—	CCI register index MSB
110	0x00	0x008B	analogue_gain_type_lo	0x06	—	Address 06xx
111	0x5A	—		0xA5	—	CCI register index LSB
112	0x00	0x008C	analogue_gain_m0_lo	0x00	—	Address xx00
113	0x5A	—		0x5A	—	auto_increment
114	0x00	0x008D	analogue_gain_m0_lo	??	0x0600	test_pattern_mode_hi
115	0x5A	—		0x5A	—	
116	0x00	0x008E	analogue_gain_c0_lo	??	0x0601	test_pattern_mode_lo
117	0x5A	—		0x5A	—	
118	0x80	0x008F	analogue_gain_c0_lo	??	0x0602	test_data_red_hi
119	0x5A	—		0x5A	—	
120	0xFF	0x0090	analogue_gain_m1_lo	??	0x0603	test_data_red_lo
121	0x5A	—		0x5A	—	
122	0xFF	0x0091	analogue_gain_m1_lo	??	0x0604	test_data_greenR_hi
123	0x5A	—		0x5A	—	
124	0x00	0x0092	analogue_gain_c1_lo	??	0x0605	test_data_greenR_lo
125	0x5A	—		0x5A	—	
126	0x80	0x0093	analogue_gain_c1_lo	??	0x0606	test_data_blue_hi
127	0xA5	—	CCI register index LSB	0x5A	—	
128	0xC0	—	Address xxC0	??	0x0607	test_data_blue_lo
129	0x5A	—	auto_increment	0x5A	—	
130	0x01	0x00C0	data_format_model_type	??	0x0608	test_data_greenB_hi
131	0x5A	—		0x5A	—	
132	0x03	0x00C1	data_format_model_subtype	??	0x0609	test_data_greenB_lo
133	0x5A	—		0x5A	—	
134	0x0A	0x00C2	data_format_descriptor_0_hi	??	0x060A	horizontal_cursor_width_hi
135	0x5A	—		0x5A	—	
136	0x0A	0x00C3	data_format_descriptor_0_lo	??	0x060B	horizontal_cursor_width_lo
137	0x5A	—		0x5A	—	
138	0x0A	0x00C4	data_format_descriptor_1_hi	??	0x060C	horizontal_cursor_position_hi
139	0x5A	—		0x5A	—	
140	0x08	0x00C5	data_format_descriptor_1_lo	??	0x060D	horizontal_cursor_position_lo
141	0x5A	—		0x5A	—	
142	0x08	0x00C6	data_format_descriptor_2_hi	??	0x060E	vertical_cursor_width_hi
143	0x5A	—		0x5A	—	
144	0x08	0x00C7	data_format_descriptor_2_lo	??	0x060F	vertical_cursor_width_lo

Offset	Row 0			Row 1		
	8-bit	Reg. Addr	Comment	8-bit	Reg. Addr	Comment
145	0x5A	—		0x5A	—	
146	0x00	0x00C8	data_format_descriptor_3_hi	??	0x0610	vertical_cursor_position_hi
147	0x5A	—		0x5A	—	
148	0x00	0x00C9	data_format_descriptor_3_lo	??	0x0611	vertical_cursor_position_lo
149	0x5A	—		0xAA	—	CCI register index MSB
150	0x00	0x00CA	data_format_descriptor_4_hi	0x07	—	Address 07xx
151	0x5A	—		0xA5	—	CCI register index LSB
152	0x00	0x00CB	data_format_descriptor_4_lo	0x00	—	Address xx00
153	0x5A	—		0x5A	—	auto_increment
154	0x00	0x00CC	data_format_descriptor_5_hi	0x05	0x0700	fifo_water_mark_pixels_hi
155	0x5A	—		0x5A	—	
156	0x00	0x00CD	data_format_descriptor_5_lo	0x10	0x0701	fifo_water_mark_pixels_lo
157	0x5A	—		0x07	—	Null Data
158	0x00	0x00CE	data_format_descriptor_6_hi	0x07	—	Null Data - up to end of line
159	0x5A	—				
160	0x00	0x00CF	data_format_descriptor_6_lo			
161	0xAA	—	CCI register index MSB			
162	0x01	—	Address 01xx			
163	0xA5	—	CCI register index LSB			
164	0x00	—	Address xx00			
165	0x5A	—	auto_increment			
166	??	0x0100	mode_select			
167	0x5A	—				
168	??	0x0101	image_orientation			
169	0x55	—	auto_increment-null data			
170	0x07	—	Null Data			
171	0x5A	—	auto_increment			
172	0x00	0x0103	software_reset			
173	0x5A	—				
174	??	0x0104	grouped_parameter_hold			
175	0x5A	—				
176	??	0x0105	mask_corrupted_frames			
177	0x55	—	auto_increment-null data			
178	0x07	0x0106	Null Data			
179	0xA5	—	CCI register index LSB			
180	0x10		Address xx10			
181	0x5A	—	auto increment			
182	0x00	0x0110	CCP2_channel_identifier			

Offset	Row 0			Row 1		
	8-bit	Reg. Addr	Comment	8-bit	Reg. Addr	Comment
183	0x5A	—				
184	??	0x0111	CCP2_signalling_mode			
185	0x5A	—				
186	??	0x0112	CCP_data_format_hi			
187	0x5A	—				
188	??	0x0113	CCP_data_format_lo			
189	0xA5	—	CCI register index LSB			
190	0x20	—	Address xx20			
191	0x5A	—	auto increment			
192	0x00	0x0120	gain_mode			
193	0xAA	—	CCI register index MSB			
194	0x02	—	Address 02xx			
195	0xA5	—	CCI register index LSB			
196	0x00	—	Address xx00			
197	0x5A	—	auto increment			
198	??	0x0200	fine_integration_time_hi			
199	0x5A	—				
200	??	0x0201	fine_integration_time_lo			
201	0x5A	—				
202	??	0x0202	coarse_integration_time_hi			
203	0x5A	—				
204	??	0x0203	coarse_integration_time_lo			
205	0x5A	—				
206	0x00	0x0204	analogue_gain_code_global_hi			
207	0x5A	—				
208	??	0x0205	analogue_gain_code_global_lo			
209	0x5A	—				
210	0x00	0x0206	analogue_gain_code_greenR_hi			
211	0x5A	—				
212	??	0x0207	analogue_gain_code_greenR_lo			
213	0x5A	—				
214	0x00	0x0208	analogue_gain_code_red_hi			
215	0x5A	—				
216	??	0x0209	analogue_gain_code_red_lo			
217	0x5A	—				
218	0x00	0x020A	analogue_gain_code_blue_hi			
219	0x5A	—				
220	??	0x020B	analogue_gain_code_blue_lo			

Offset	Row 0		
	8-bit	Reg. Addr	Comment
221	0x5A	—	
222	0x00	0x020C	analogue_gain_code_greenB_hi
223	0x5A	—	
224	??	0x020D	analogue_gain_codegreenB_lo
225	0x5A	—	
226	??	0x020E	digital_gain_greenR_hi
227	0x5A	—	
228	0x00	0x020F	digital_gain_greenR_lo
229	0x5A	—	
230	??	0x0210	digital_gain_red_hi
231	0x5A	—	
232	0x00	0x0211	digital_gain_red_lo
233	0x5A	—	
234	??	0x0212	digital_gain_blue_hi
235	0x5A	—	
236	0x00	0x0213	digital_gain_blue_lo
237	0x5A	—	
238	??	0x0214	digital_gain_greenB_hi
239	0x5A	—	
240	0x00	0x0215	digital_gain_greenB_lo
241	0x07	—	Null Data
242	0x07	—	Null Data - up to end of line

Row 1		
8-bit	Reg. Addr	Comment

IMPORTANT NOTICE

For More Information
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